

Compal Confidential

NAV70 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRIII

2010-05-19

REV: 1.0
(Cost down)

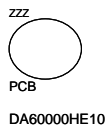
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	SCHEMATIC MB A6222
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File Name : LA-6222P

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GEN1

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INT MIC

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MIC Jack

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89V	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 17)

	VCC	3.3V				
	Ra	100K				
	ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max
NAV50	0	R01 (EVT)	0	0V	0V	0V
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V
	3	R10A (MP)	33K	0.712V	0.819V	0.875V
NAV60	4	R01 (EVT)	56K	1.036V	1.185V	1.264V
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V
	7	R10A (MP)	NC	2.500V	3.3V	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

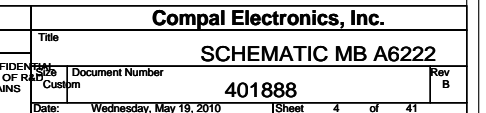
EC SM Bus2 address

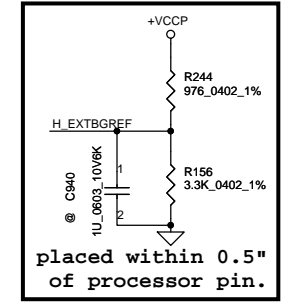
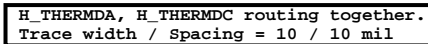
Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

ICH7M SM Bus address

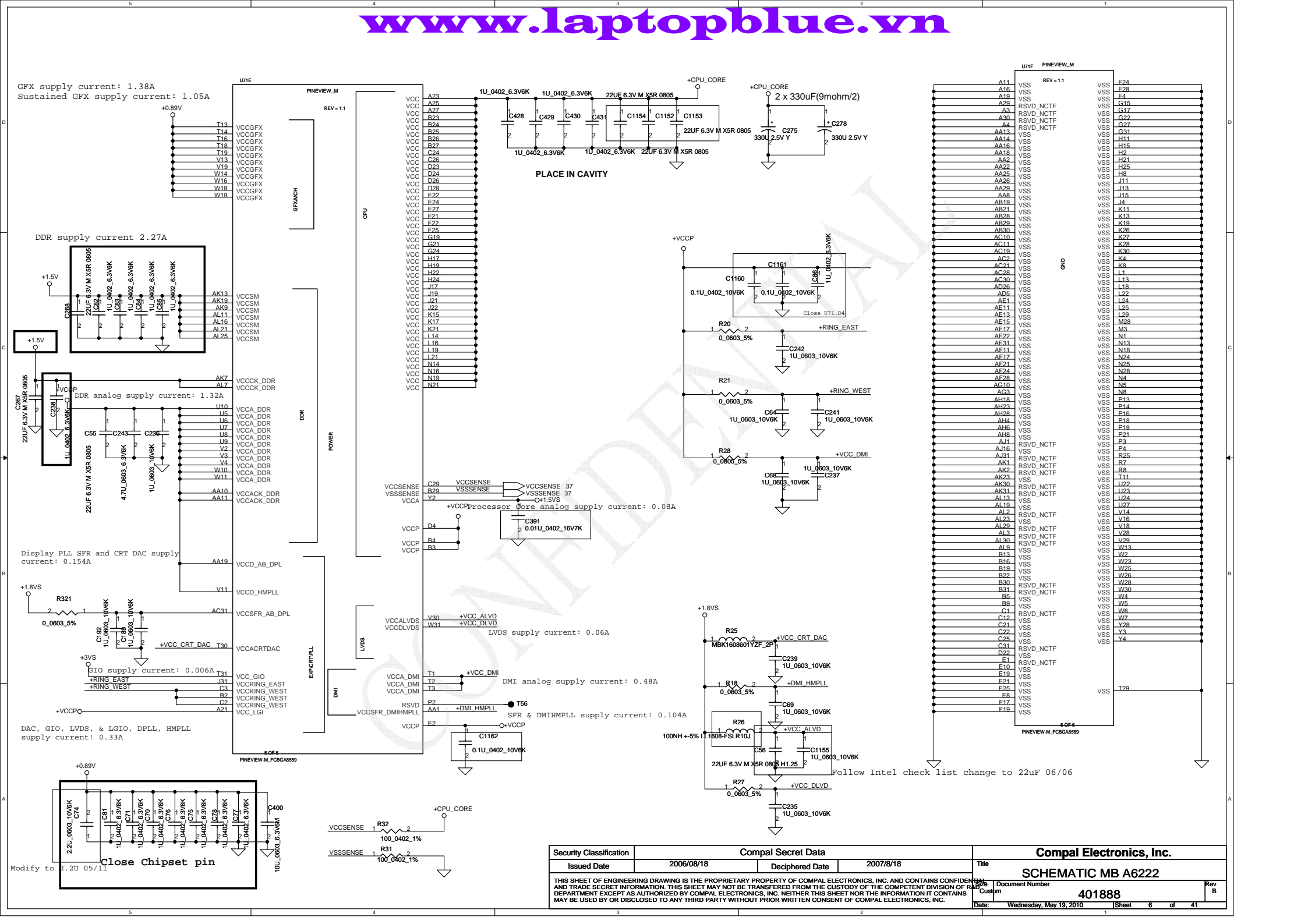
Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

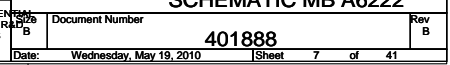
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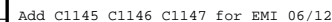
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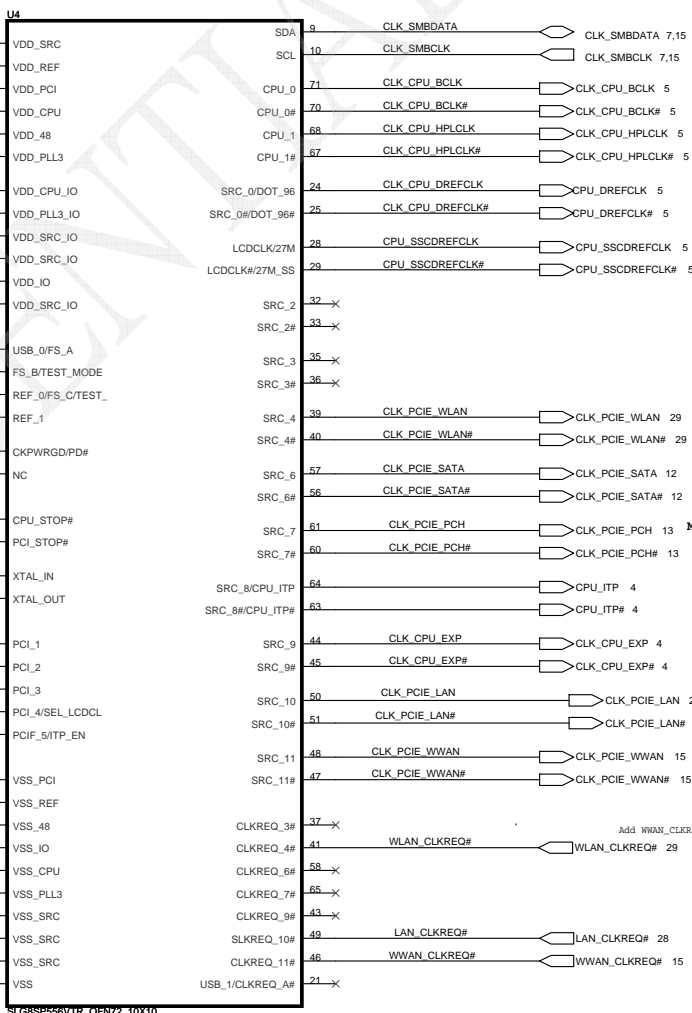
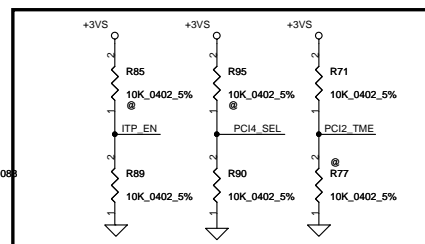
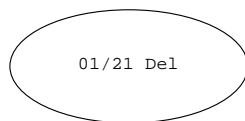
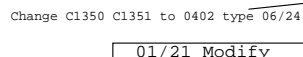
Change C174 C175 to 10U_0603 05/14

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+3VS ○ 1 2

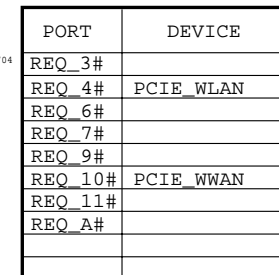


Realtek: SA00003H730



PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

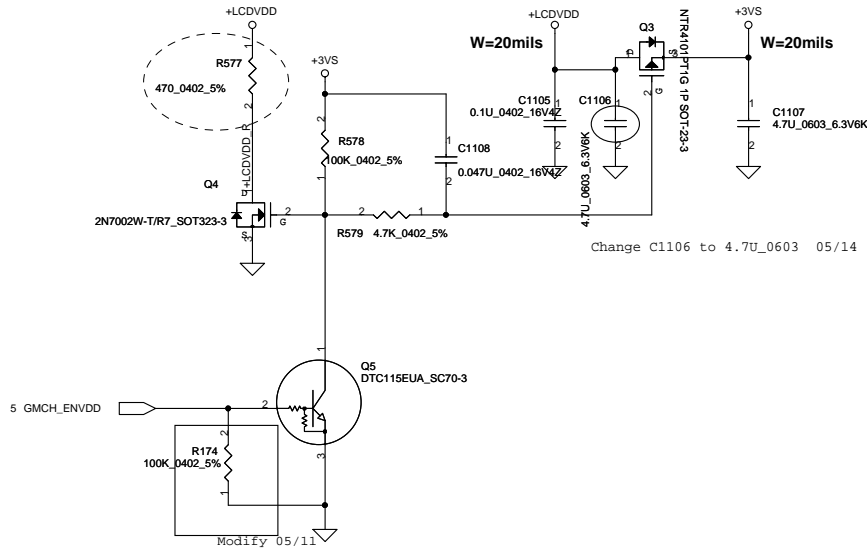
2 Modify CLK SRC Port list 05/12



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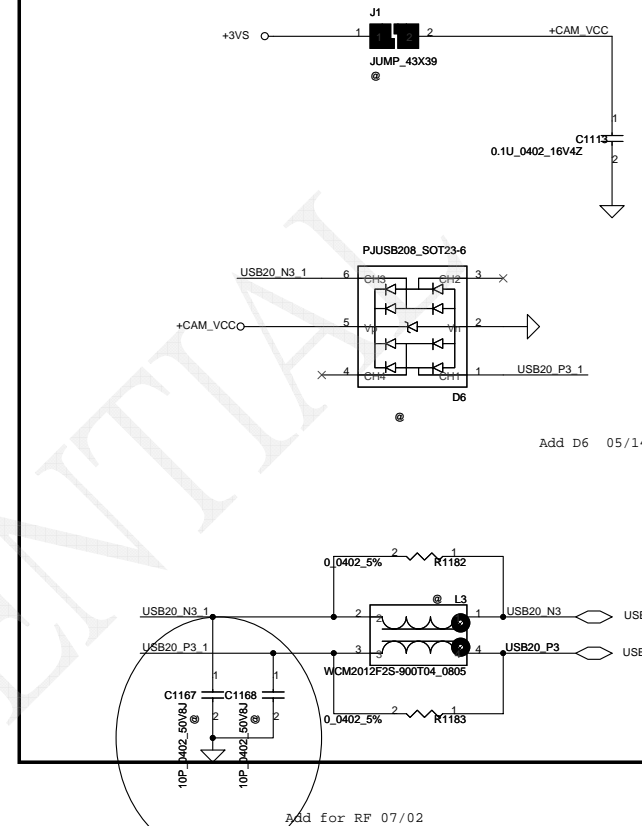
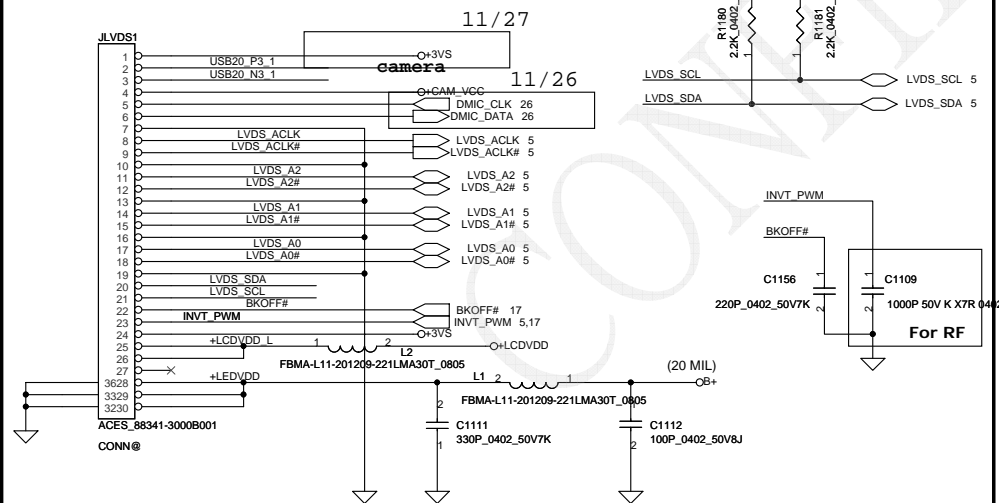
LCD POWER CIRCUIT

Change R577 to 0402 SIZE 06/16

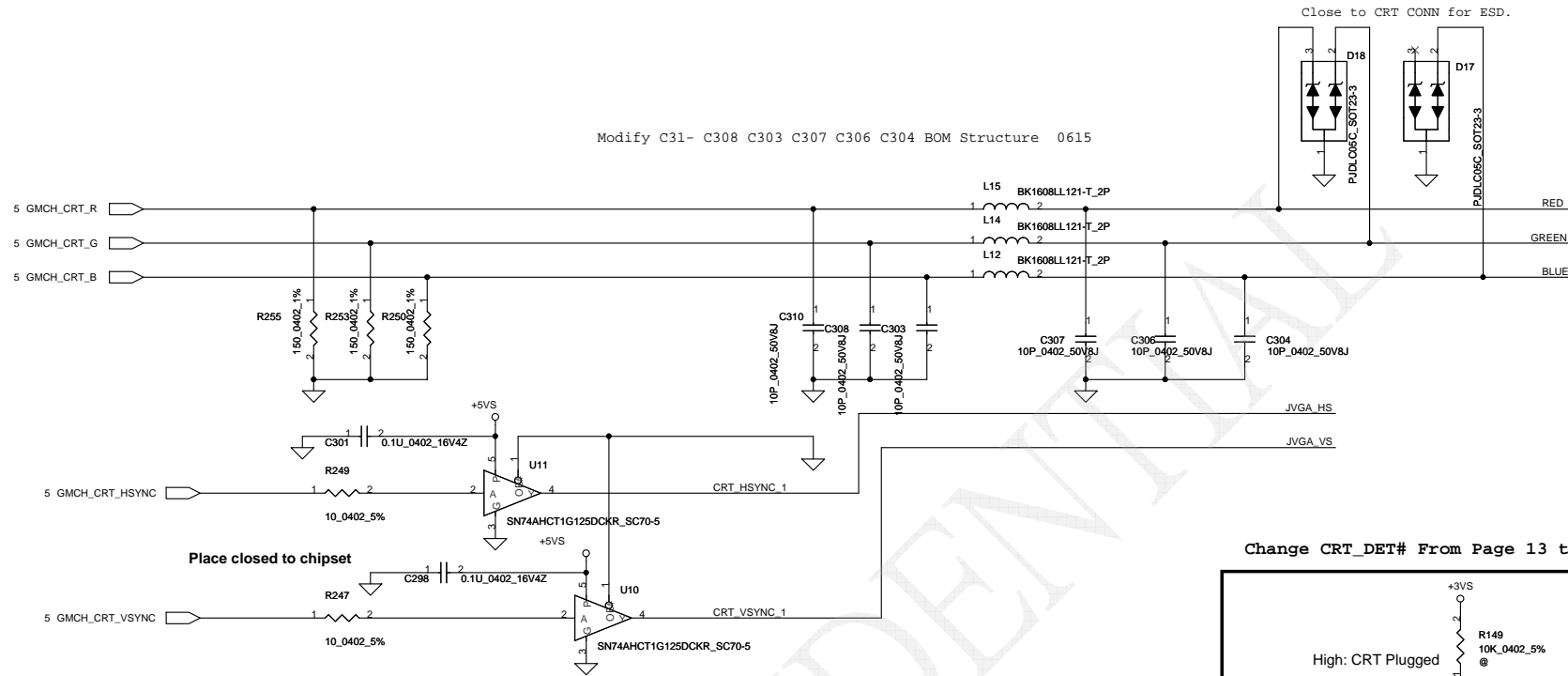


CMOS & LCD/PANEL BD. Conn.

Modify JLVDS1 08/04

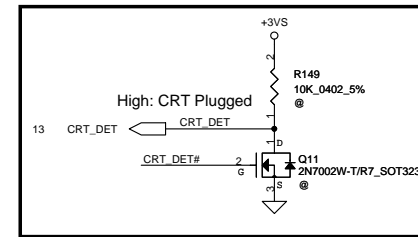


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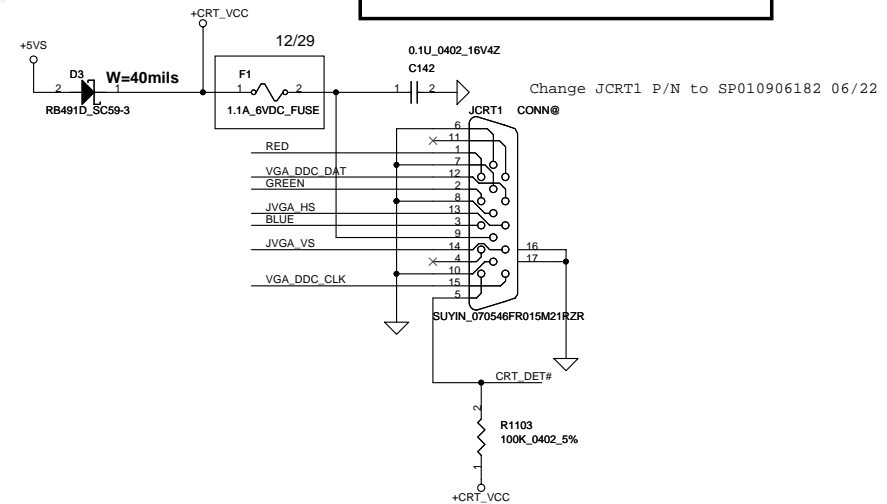
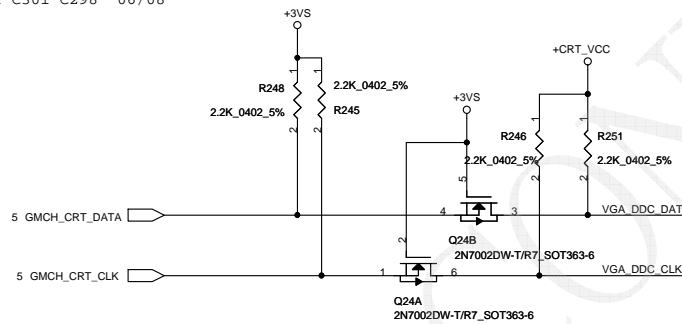


Add R1283 R1284
Change R247 R249 to 10 ohm
Add @ on U10 U11 C301 C298 06/08

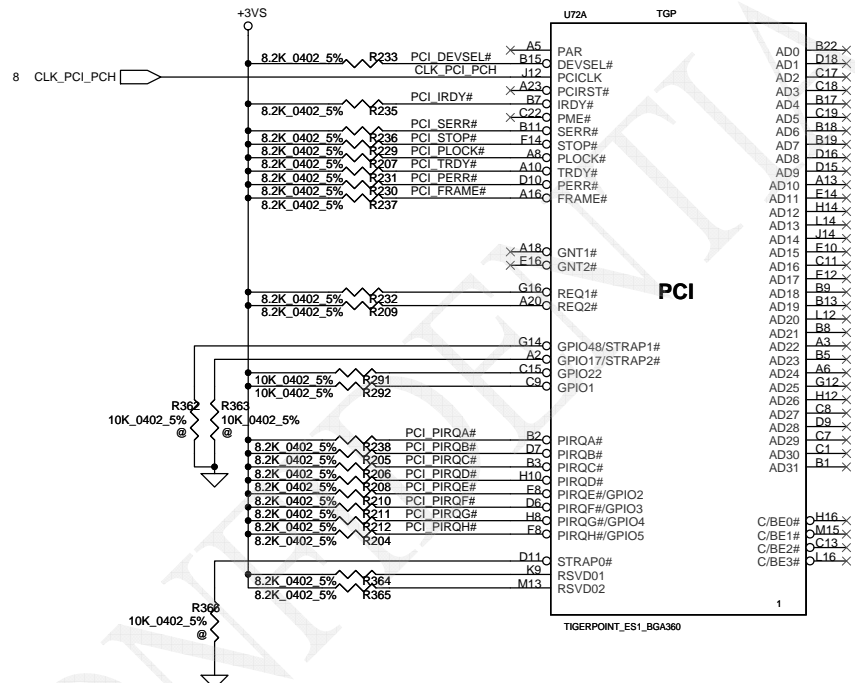
Change CRT_DET# From Page 13 to Page 10 06/12



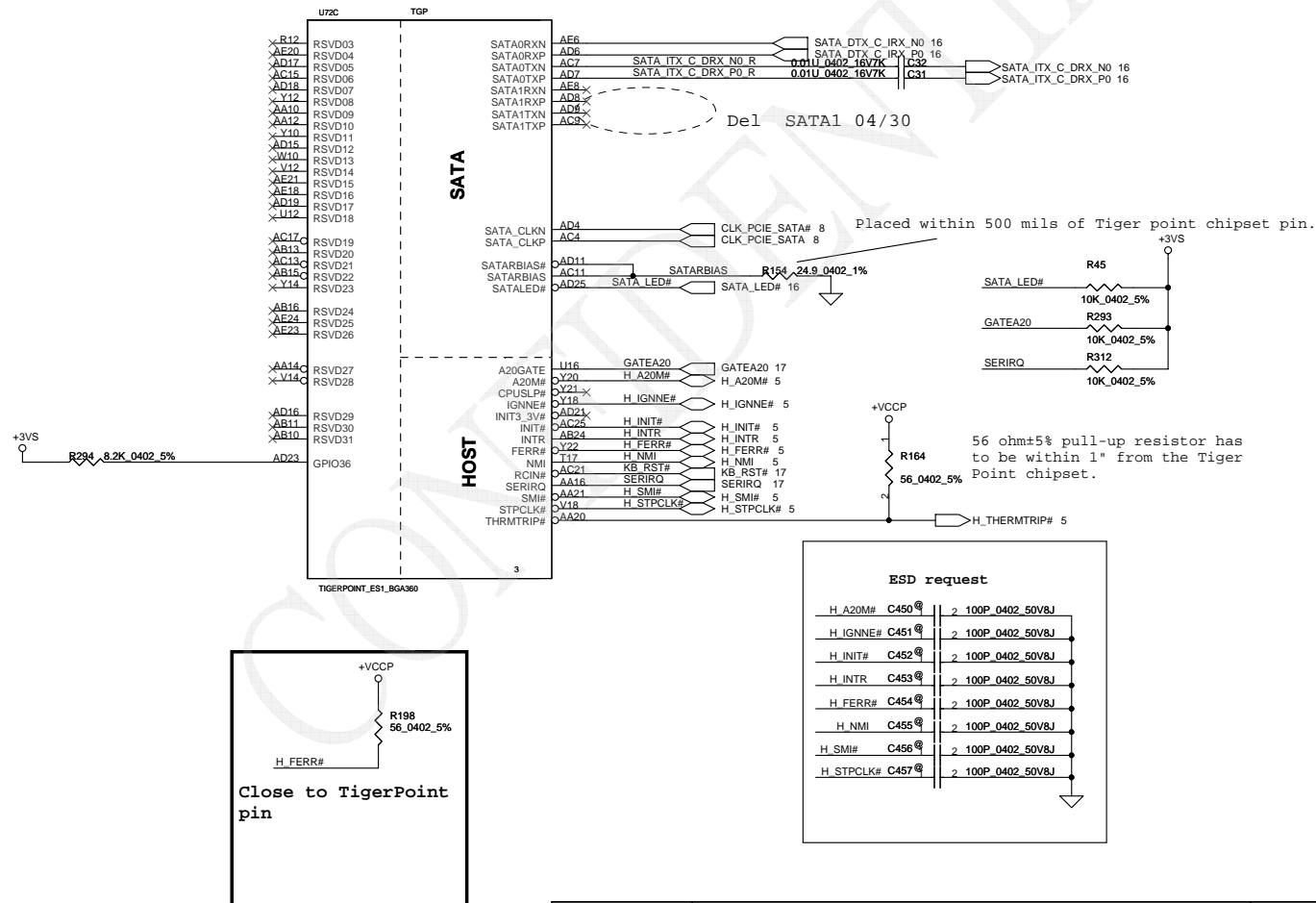
CRT PORT



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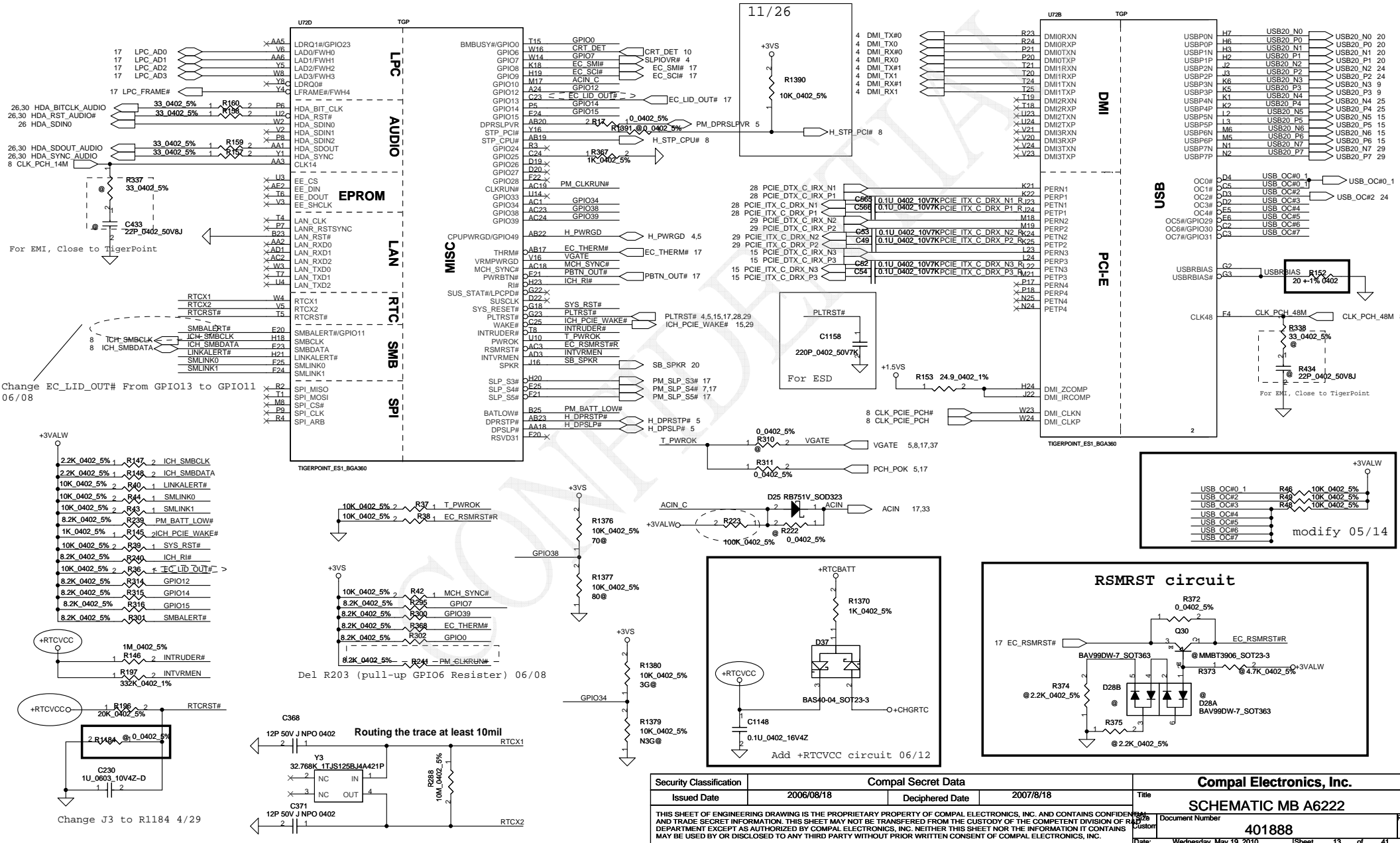
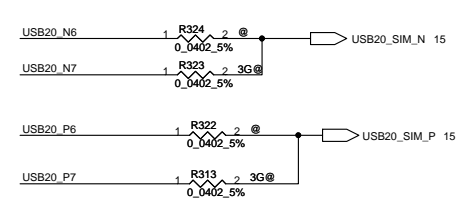
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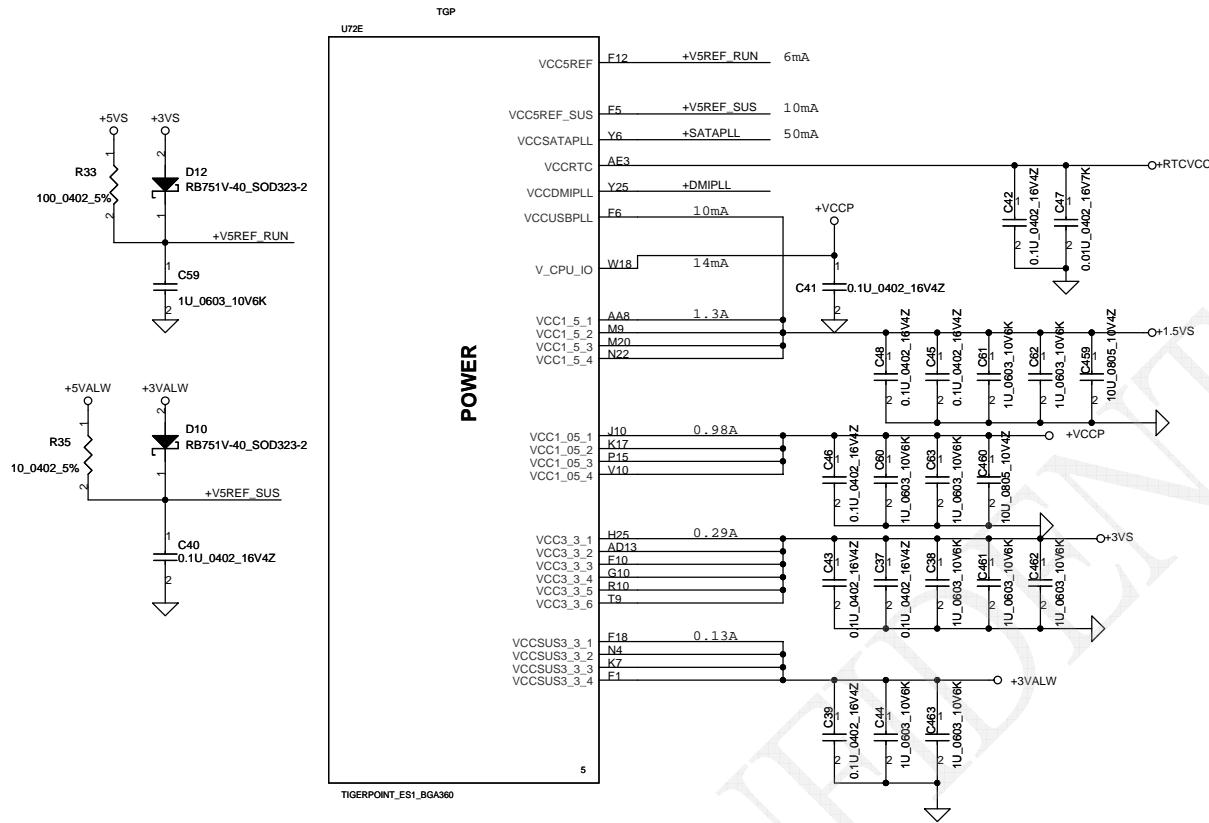
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PCIE Port List	
1	LAN
2	WLAN
3	WWAN
4	WIMAX

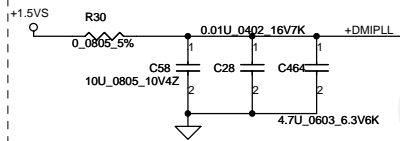
USB Port List	
0	USB Left1
1	USB Left2
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX



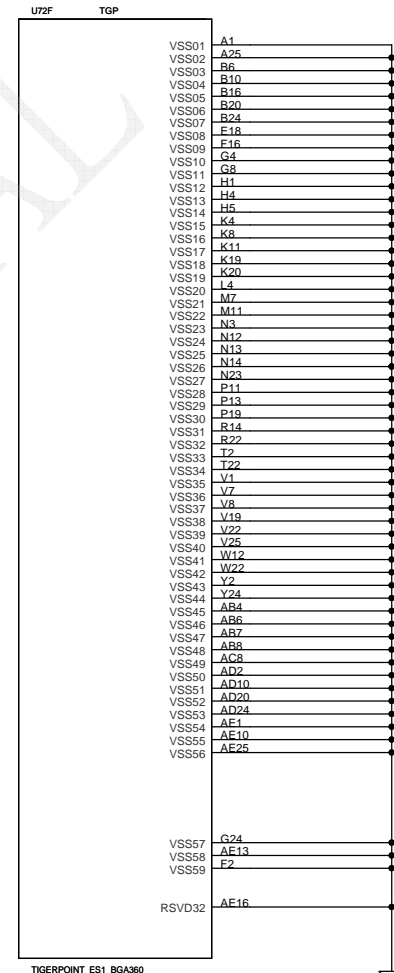
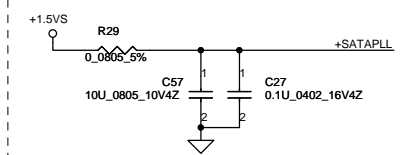
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Place closely pin Y25 within 100mlis.



Place closely pin Y6 within 100mlis.



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Mini-Express Card for WWAN

17 EC_TX_P80_DATA
17 EC_RX_P80_CLK

EC_TX_P80_DATA
EC_RX_P80_CLK

R402, 0402, 5%
R403 0.0402, 5%

Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T 06/29

13,29 ICH_PCIE_WAKE# ICH_PCIE_WAKE#

8 WWAN_CLKREQ# WWAN_CLKREQ#

8 CLK_PCIE_WWAN#
8 CLK_PCIE_WWAN

Change to PCIE_P3 05/13

13 PCIE_DTX_C_IRX_N3

13 PCIE_DTX_C_IRX_P3

13 PCIE_ITX_C_DRX_N3

13 PCIE_ITX_C_DRX_P3

+3VS_WWAN

10U_0805_10V4Z

WWAN_WAKEUP_R#

UIM_VPP

UIM_DATA

UIM_RST

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

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UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

UIM_DATA

UIM_PWR

UIM_CLK

UIM_RST

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UIM_CLK

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UIM_DATA

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UIM_CLK

UIM_RST

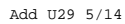
UIM_DATA

UIM_PWR

</

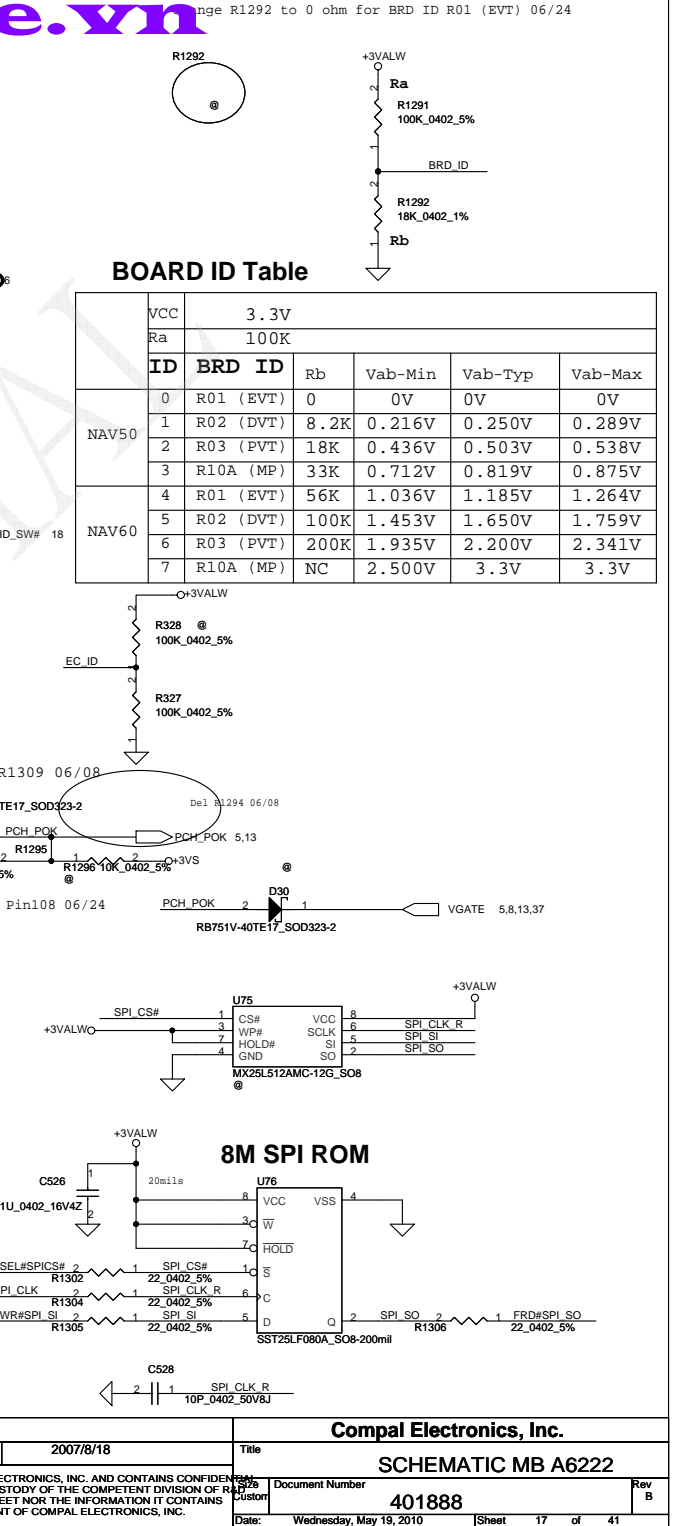
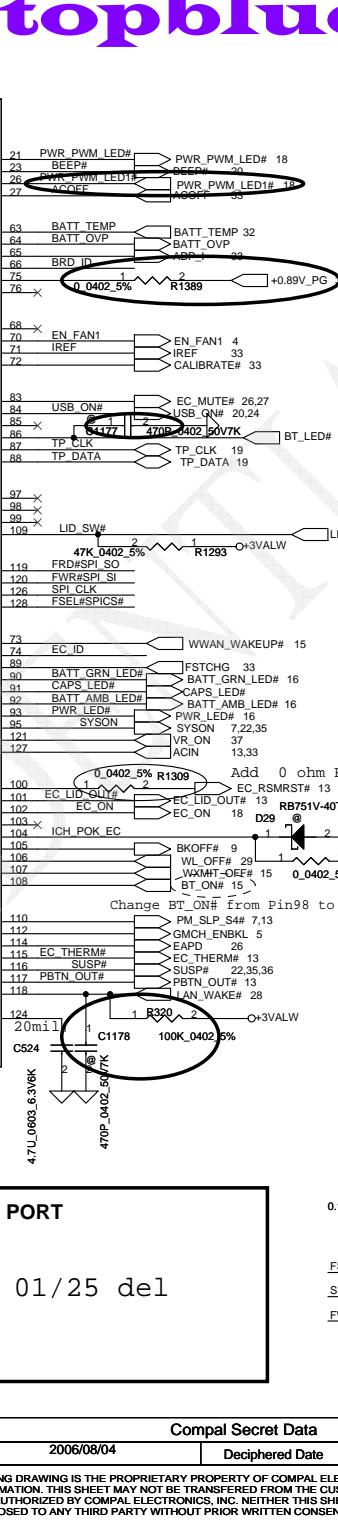
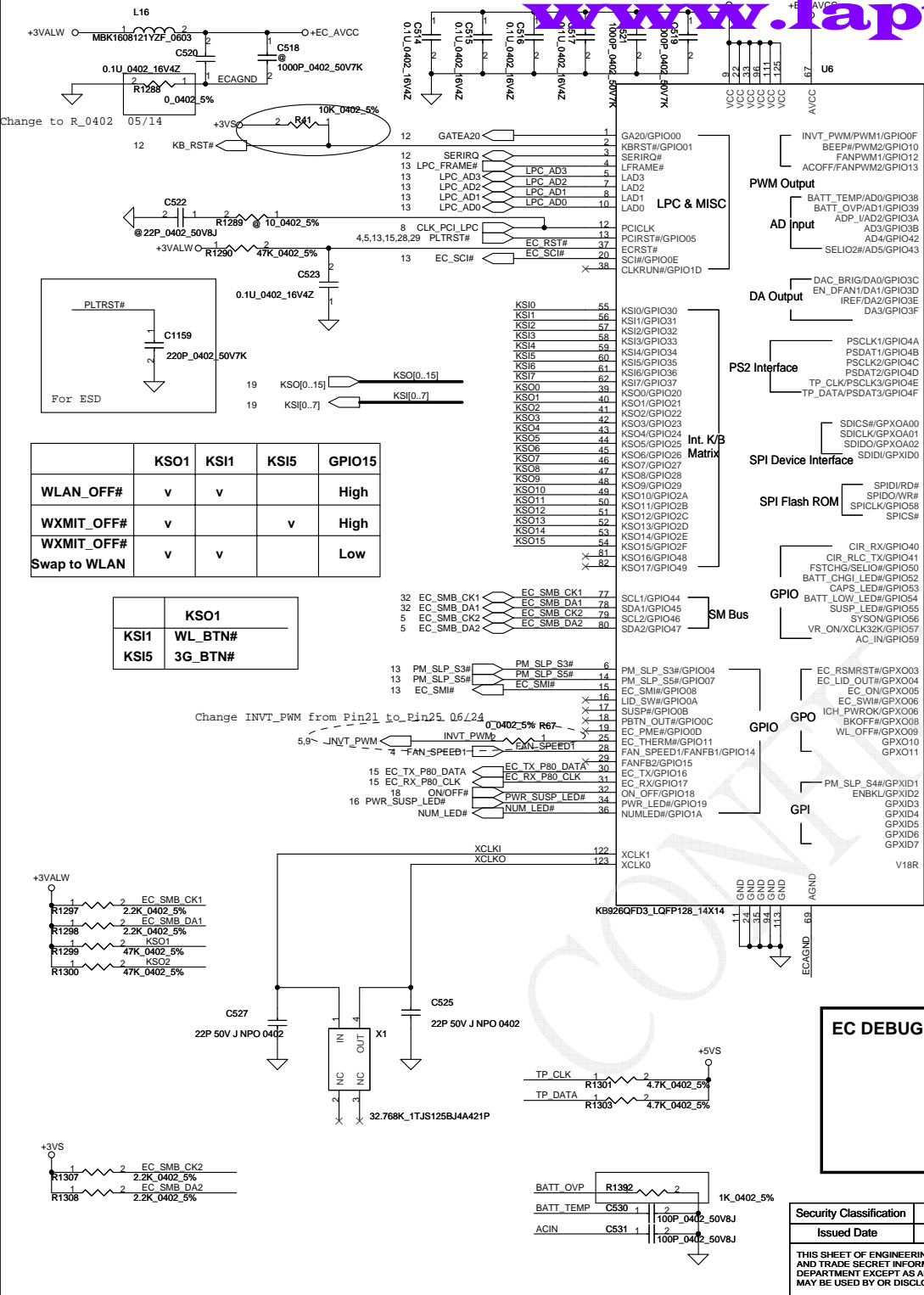
LED PCB CONN

09/03 Change +5VALW , +5VS to +3VALW +3VS



CONN@

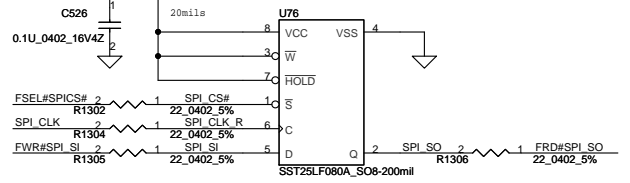
Date: Wednesday, May 19, 2010 Sheet 16 of 41



BOARD ID Table

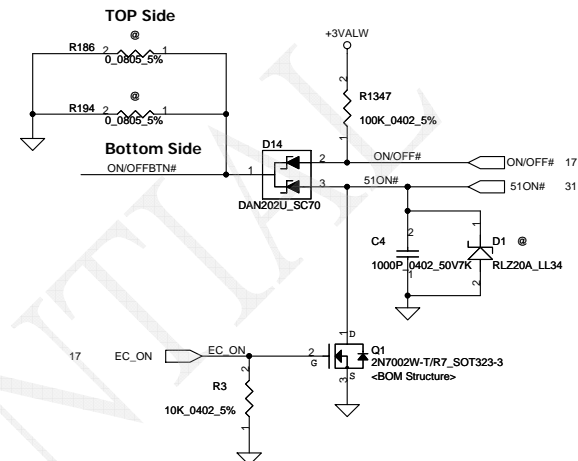
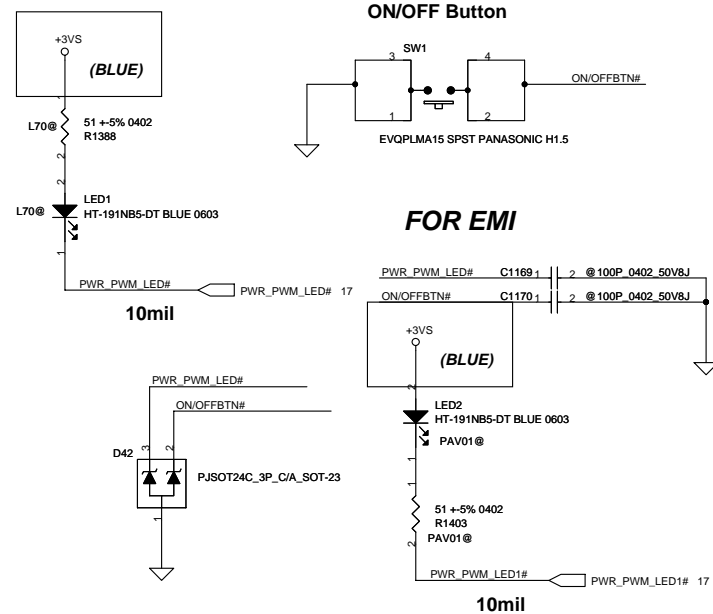
ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max
0	R01 (EVT)	0	0V	0V	0V
1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V
2	R03 (PVT)	18K	0.436V	0.503V	0.538V
3	R10A (MP)	33K	0.712V	0.819V	0.875V
4	R01 (EVT)	56K	1.036V	1.185V	1.264V
5	R02 (DVT)	100K	1.453V	1.650V	1.759V
6	R03 (PVT)	200K	1.935V	2.200V	2.341V
7	R10A (MP)	NC	2.500V	3.3V	3.3V

8M SPI ROM



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						401888					
						Date: Wednesday, May 19, 2010		Sheet 17 of 41			

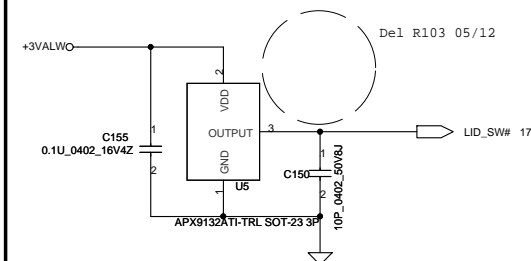
Add For NAV50 07/06
09/03 Change +5VS to +3VS



PWR/B Conn

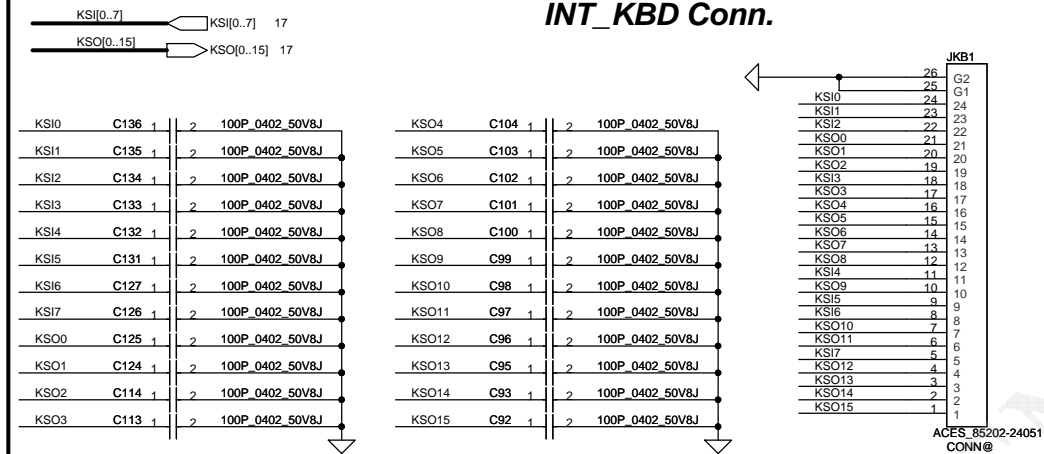
DEL PW/B Conn 0125

LID Switch

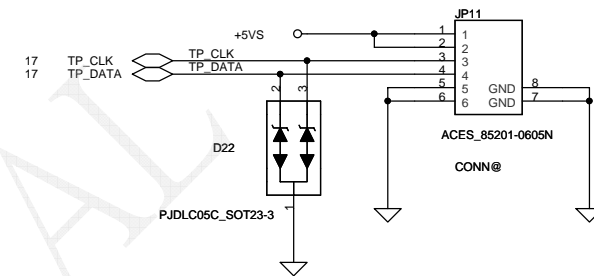


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INT_KBD Conn.



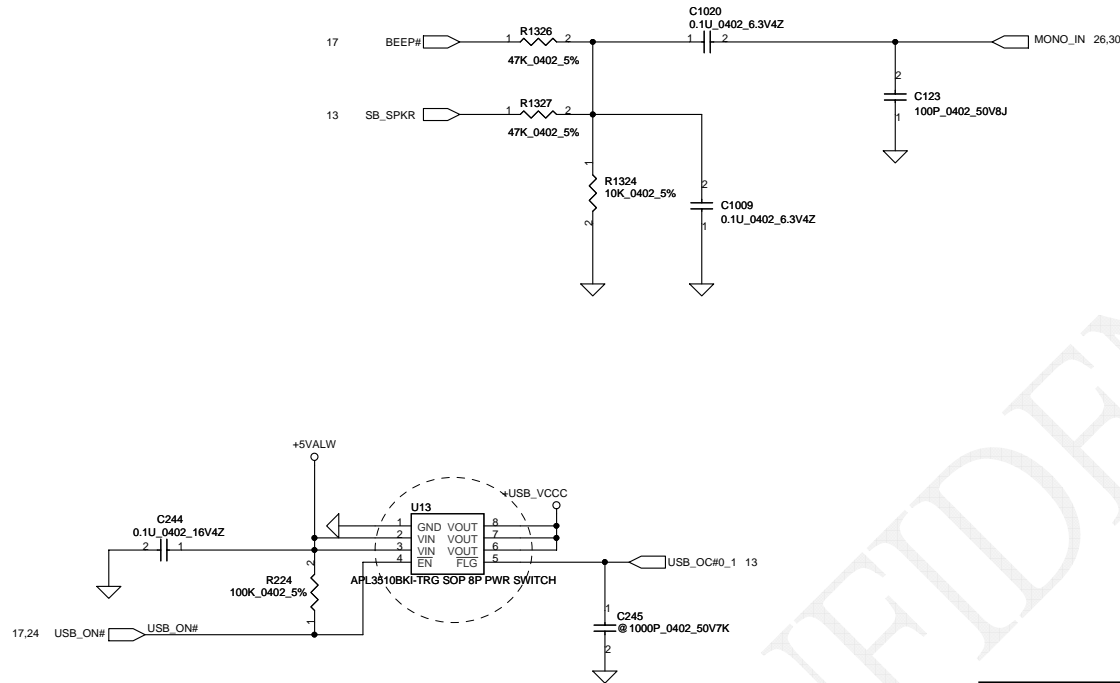
To TP/B Conn.



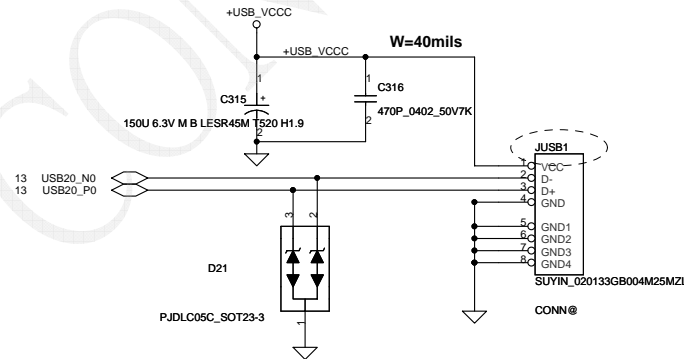
Chage JP11 Pin define & Add D22 05/14

Update TP/B Conn 05/04

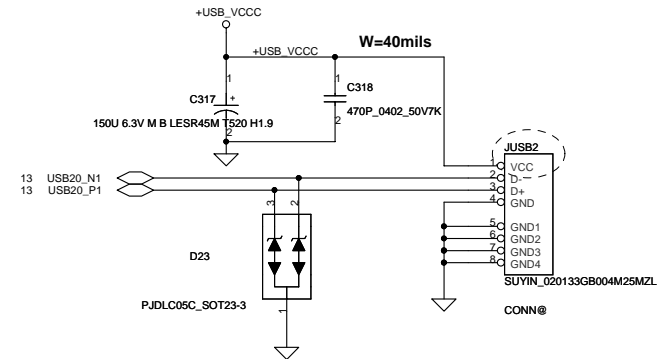
6/26 Add circuit



USB CONN.1

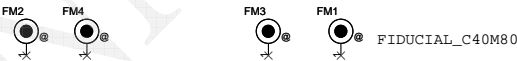
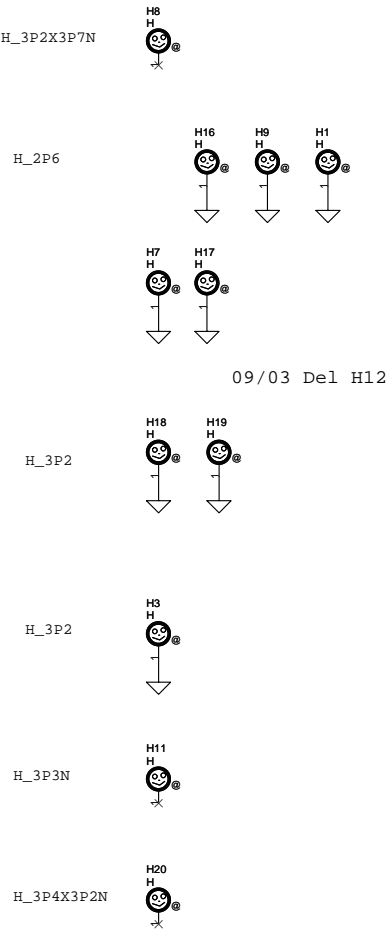


USB CONN.2



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								SCHEMATIC MB A6222	
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				Sheet		20		of 41	

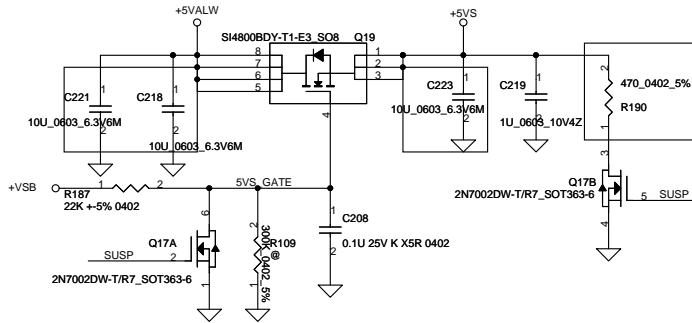
Modify Hole location by (ME Drawing 06/12) 0615



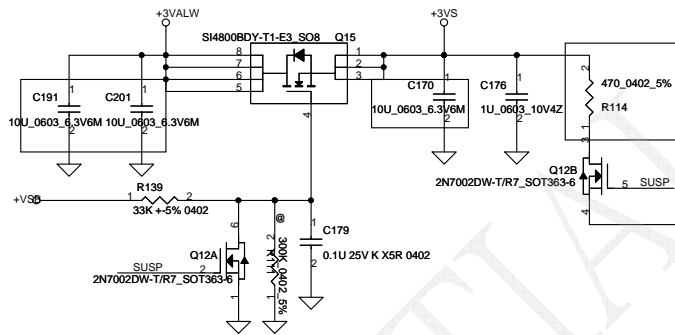
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	SCHEMATIC MB A6222
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Change R51 R57 R70 R63 R317 R114 R190 to 0402 SIZE 04/30
Change C221 C218 C223 C 191 C201 C170 C392 C393 C394 to 0603 SIZE 04/30

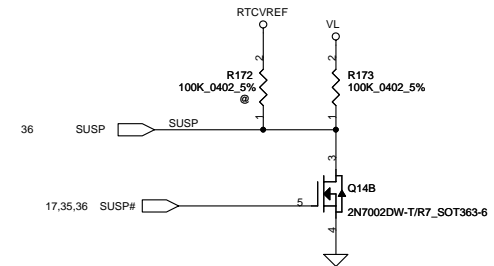
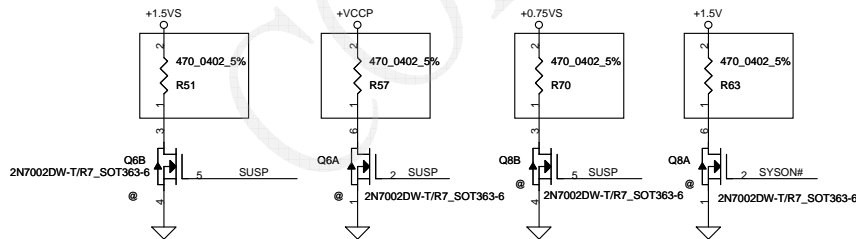
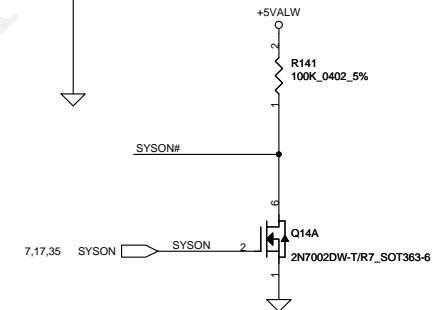
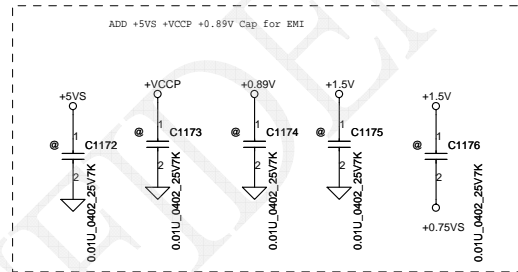
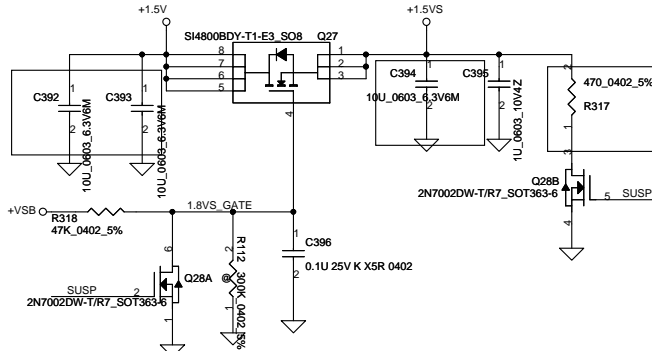
+5VALW TO +5VS



+3VALW TO +3VS



+1.5V to +1.5VS



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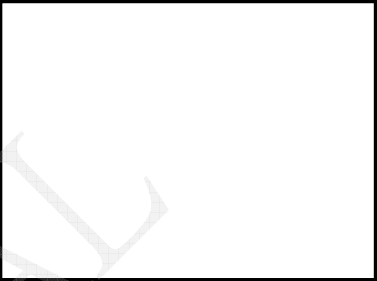
SCHEMATIC MB A6222

COMPAL CONFIDENTIAL

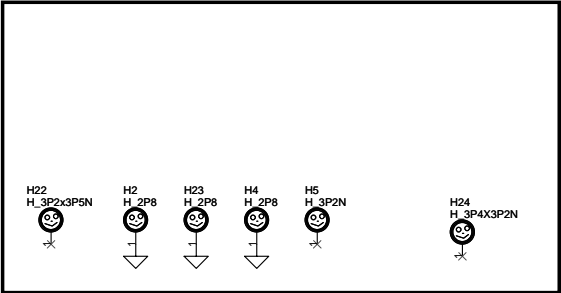
www.laptopblue.vn

MODEL NAME: NAV50
PCB NAME: LS-5655P I/O Board
COMPAL P/N: DA60000FF30
REVISION: 3.0
DATE: 2009/12/01

5/5 Update compal number



8/6 Update information about aperture

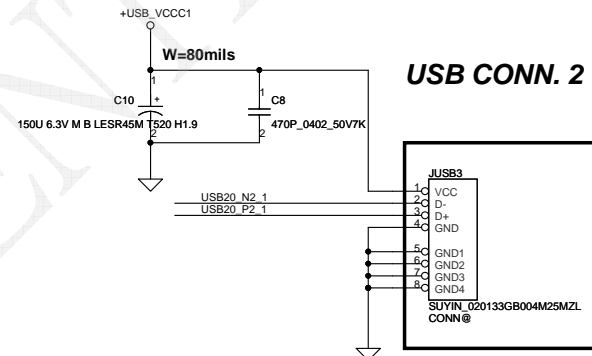
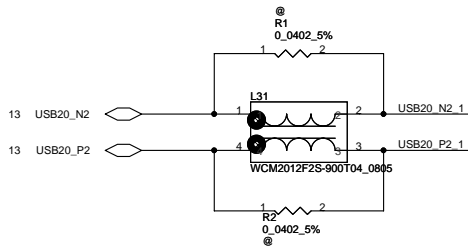
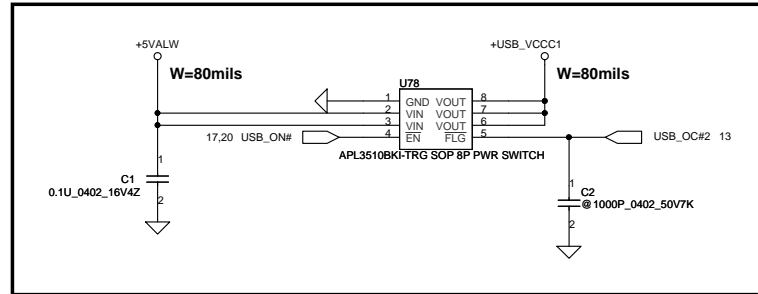


5/20 Update connector pin name
6/23 Update connector pin name
7/01 Update pin number 8,10,14,16,20,22
7/02 Update PIN42 to +5VS

CONFIDENTIAL

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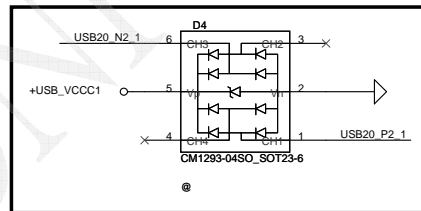
5/5 Add U2 circuit



USB CONN. 2

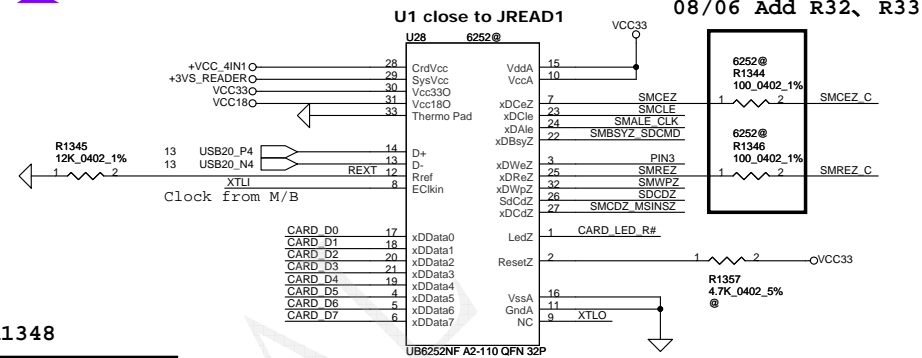
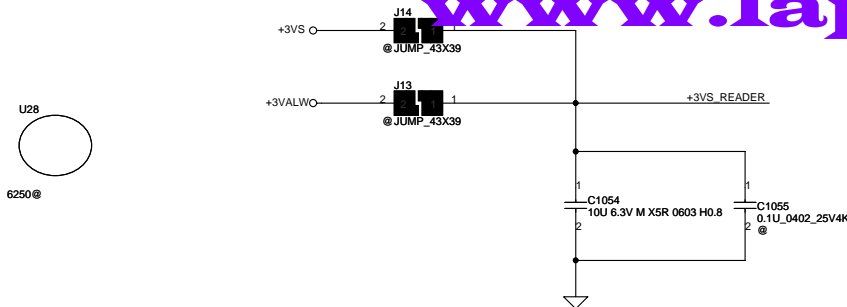
5/12 Revised USB connector
6/23 Update USB connector

5/12 Revised net name

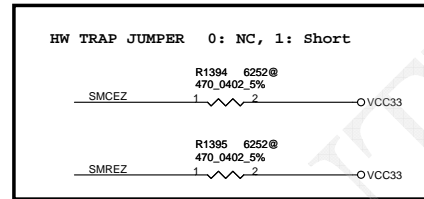


5/14 Deleted JUSB2

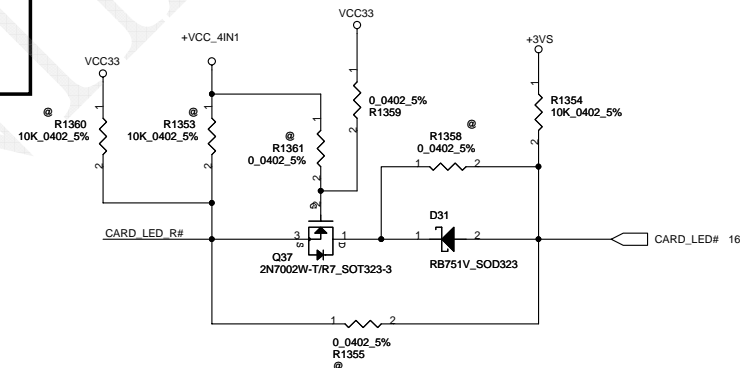
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08/06 Add R1347, R1348

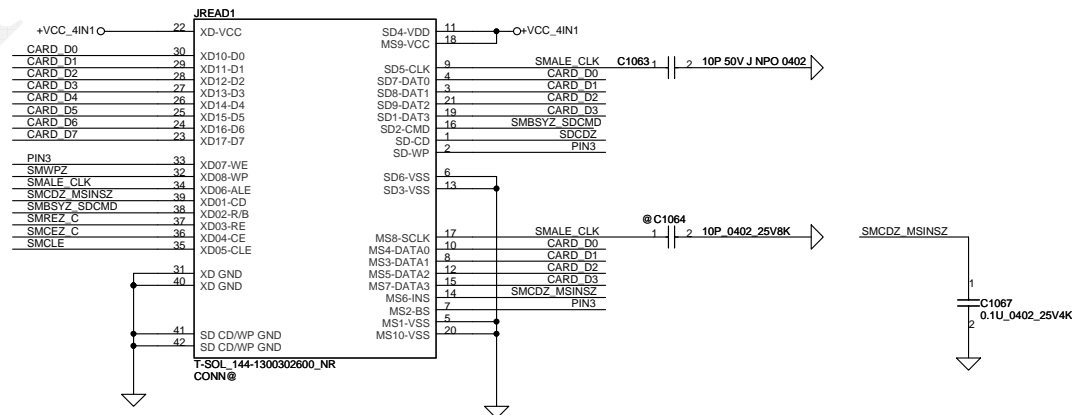


If use external crystal(Y4),
U1 will change UB6252

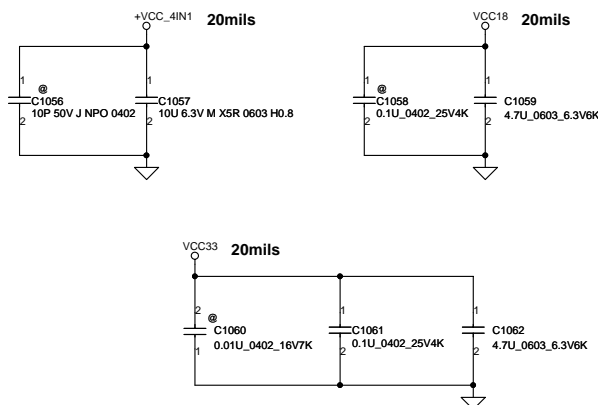


07/02 Update JREADER1

Card Reader Connector



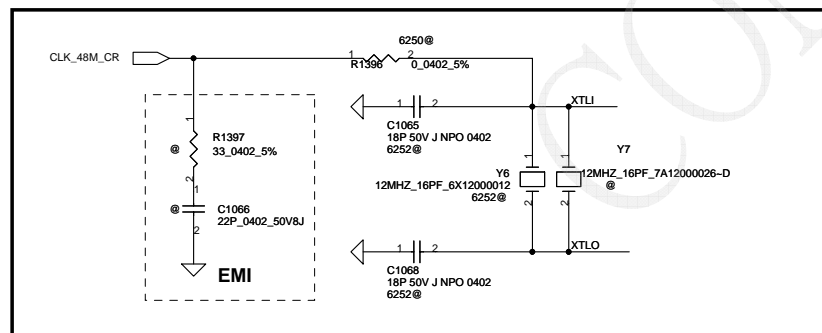
C1048, C1049 close to U1



07/02 Revised C1053 to 0.01u

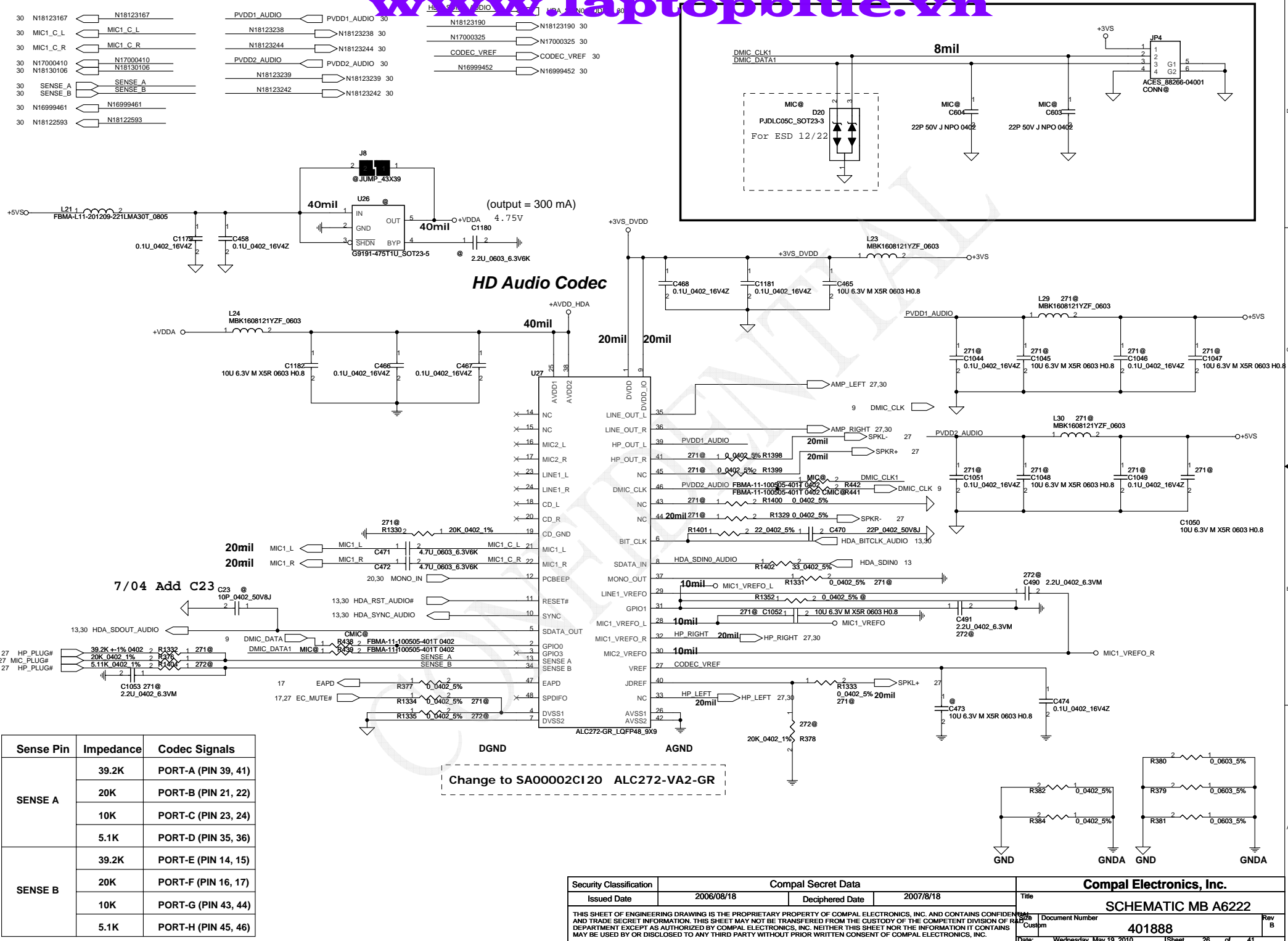
ByPass Capacitors

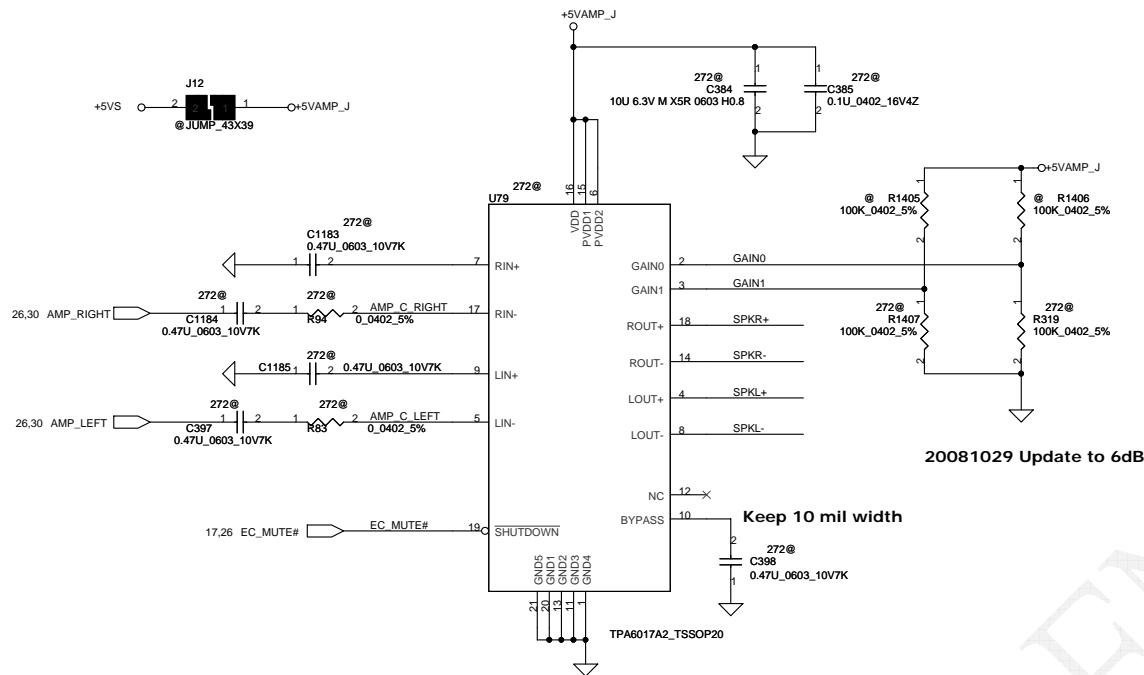
4/30 Add CLK_SD_48M



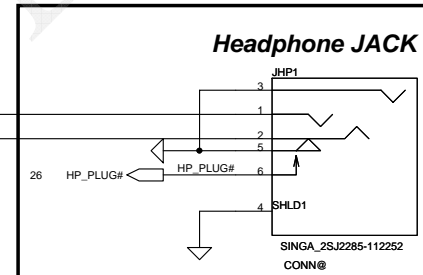
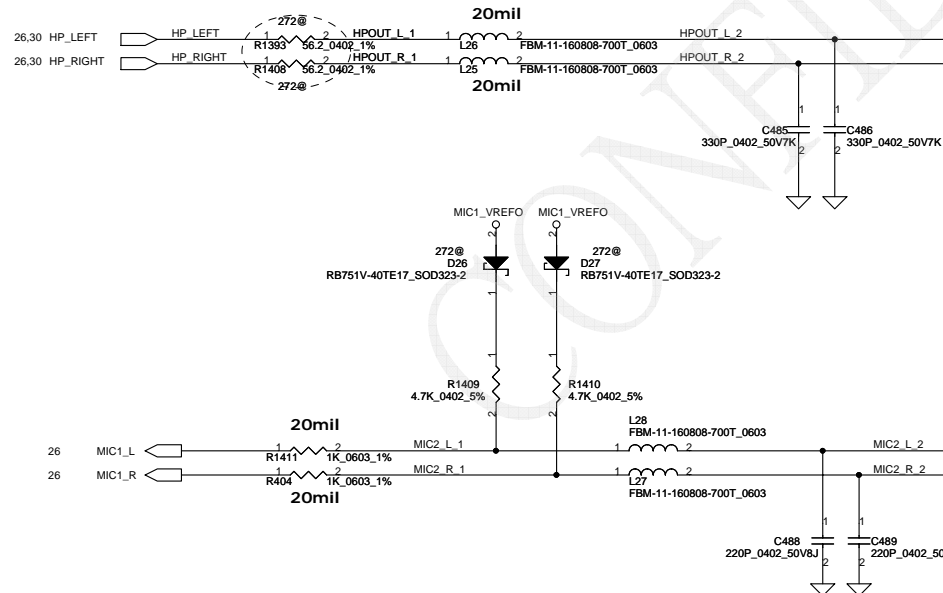
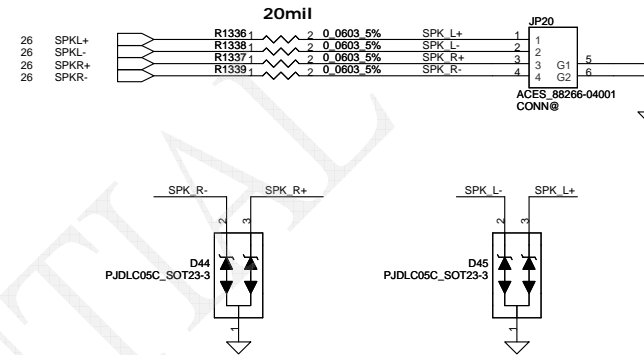
Only UB6252
need to use XTLO and XTLO

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								Document Number		401888		Rev B	
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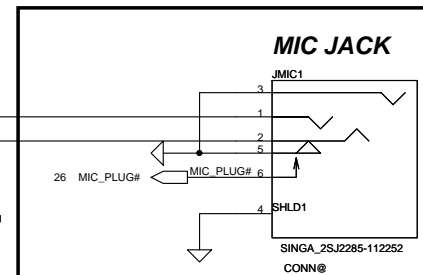




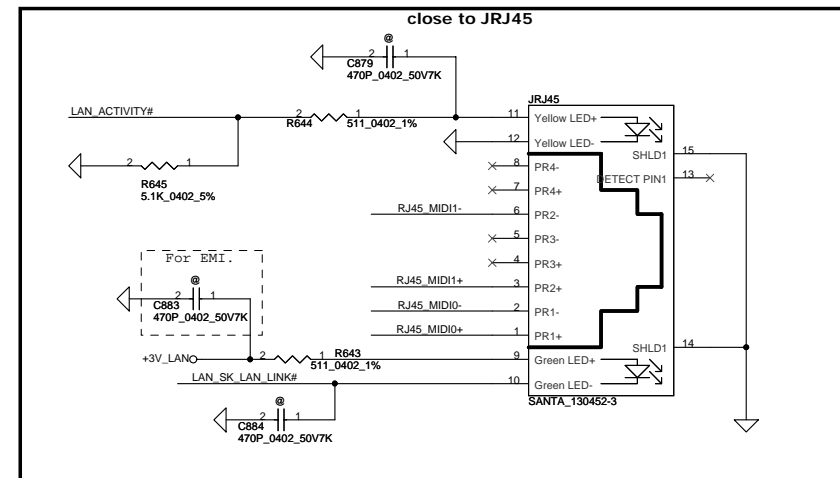
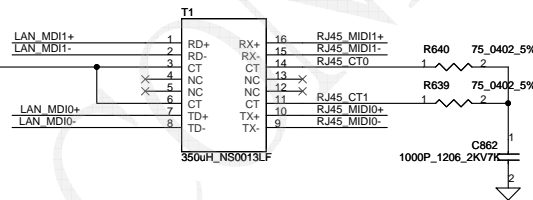
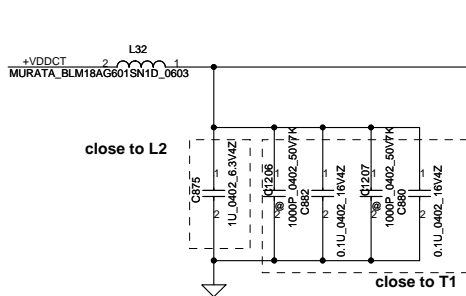
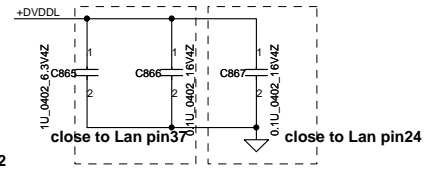
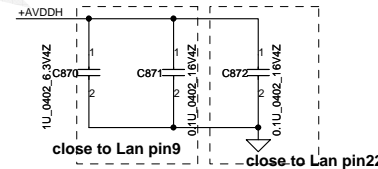
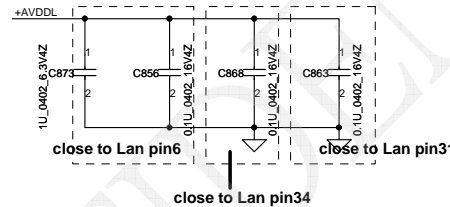
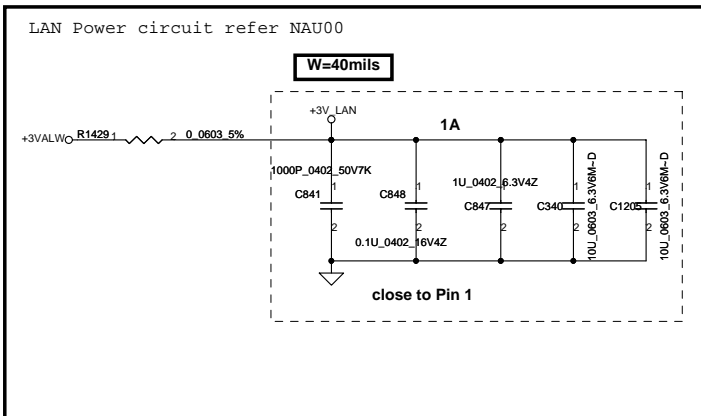
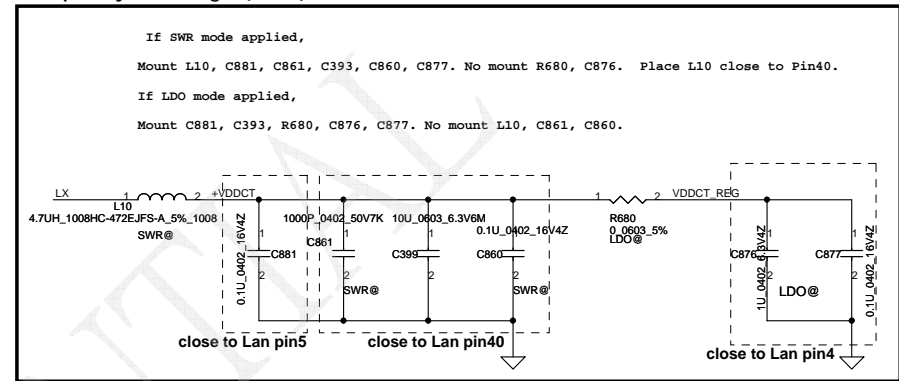
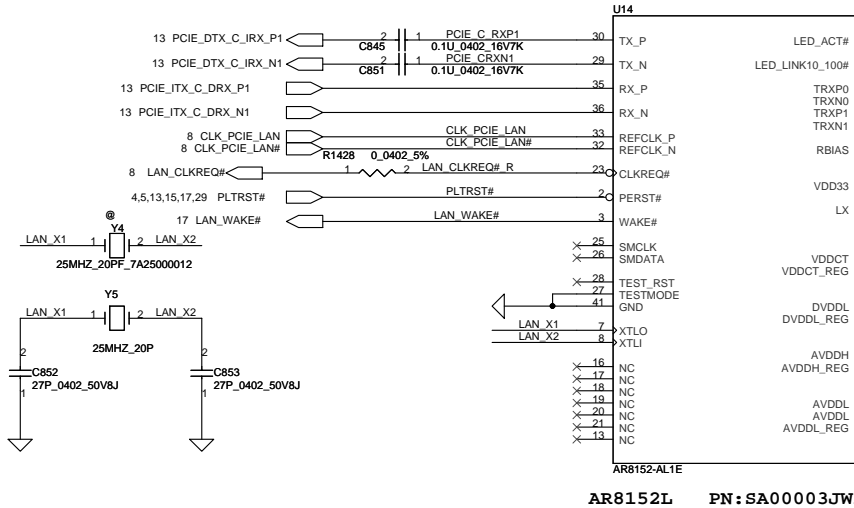
Int. Speaker Conn.



6/19 Update Headphone connector

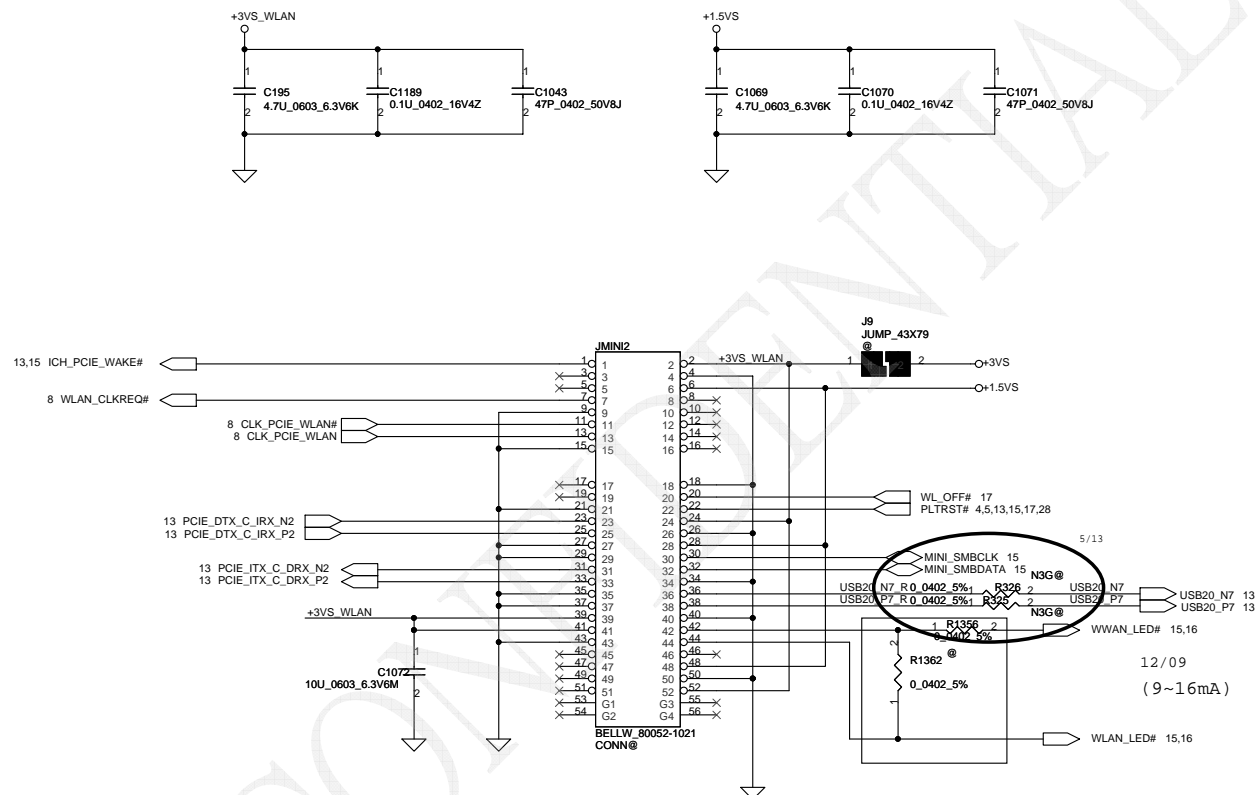


6/19 Update MIC connector



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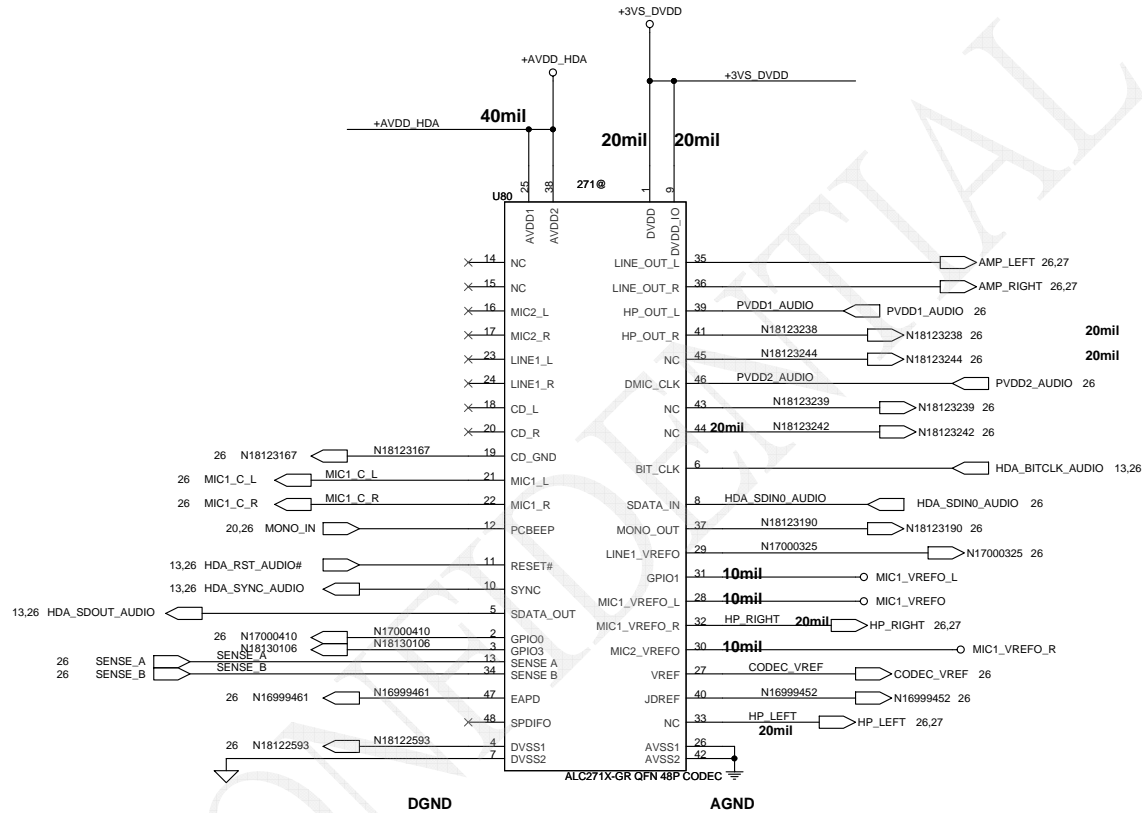
Mini-Express Card for WLAN



5/12 Update WLAN connector(the same as KAV60)
6/1 Revised 37, 39, 41, 42, 43 to NC
6/12 Update connector to DC040006S00
6/26 Update JMINI1 footprint
7/01 update pin 23,25,31,33

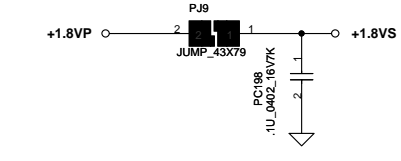
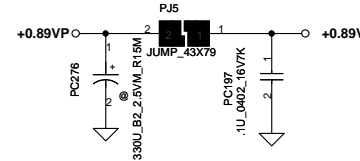
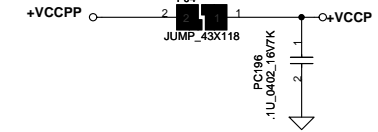
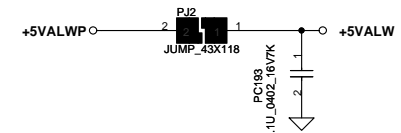
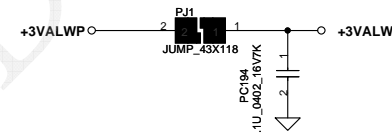
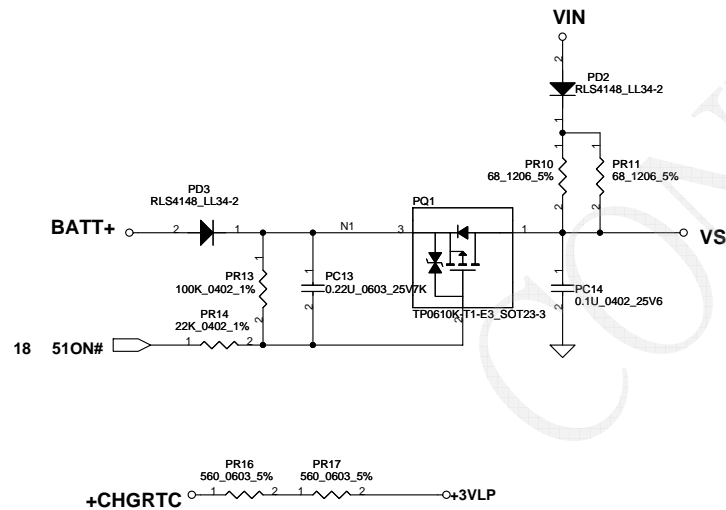
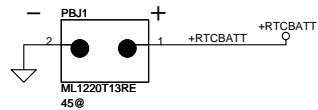
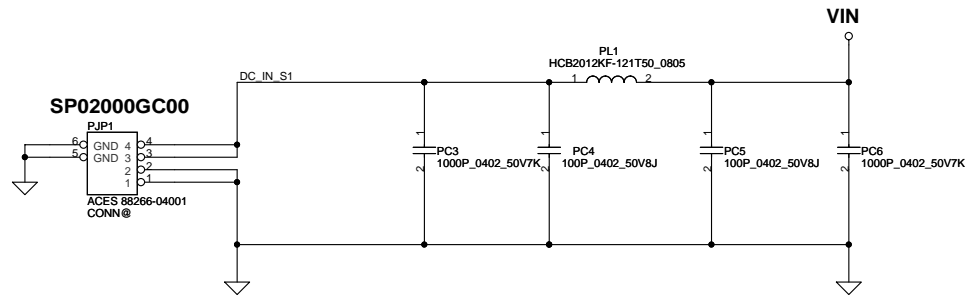
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				Custom	
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HD Audio Codec



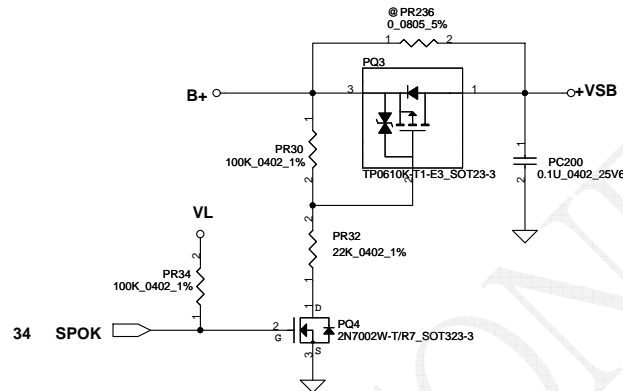
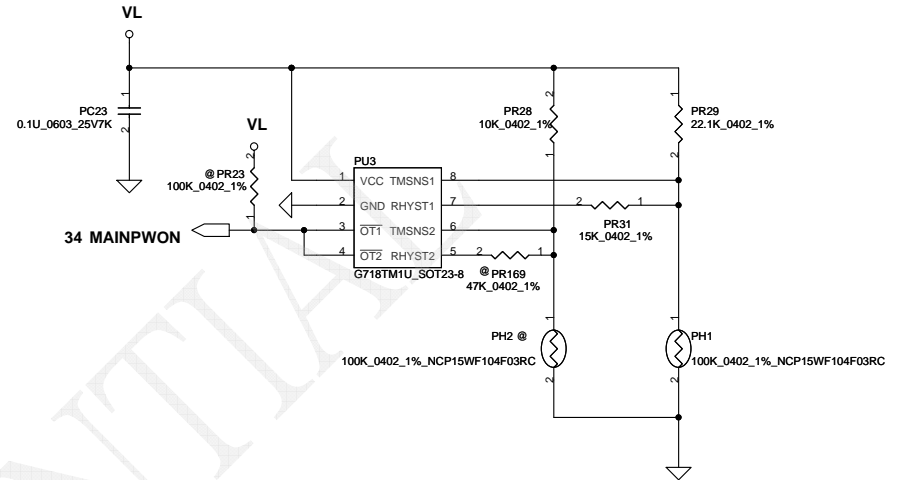
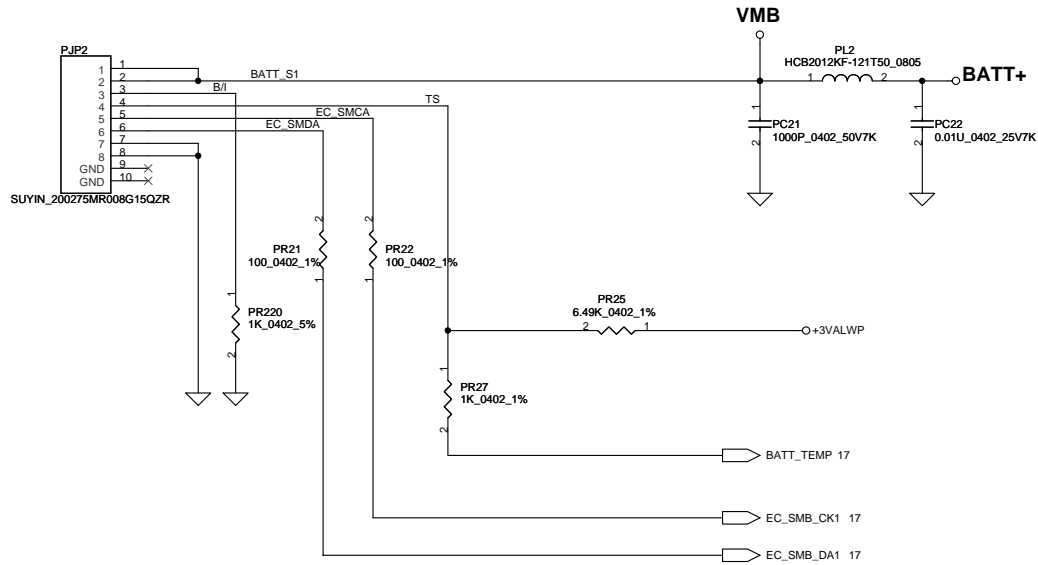
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

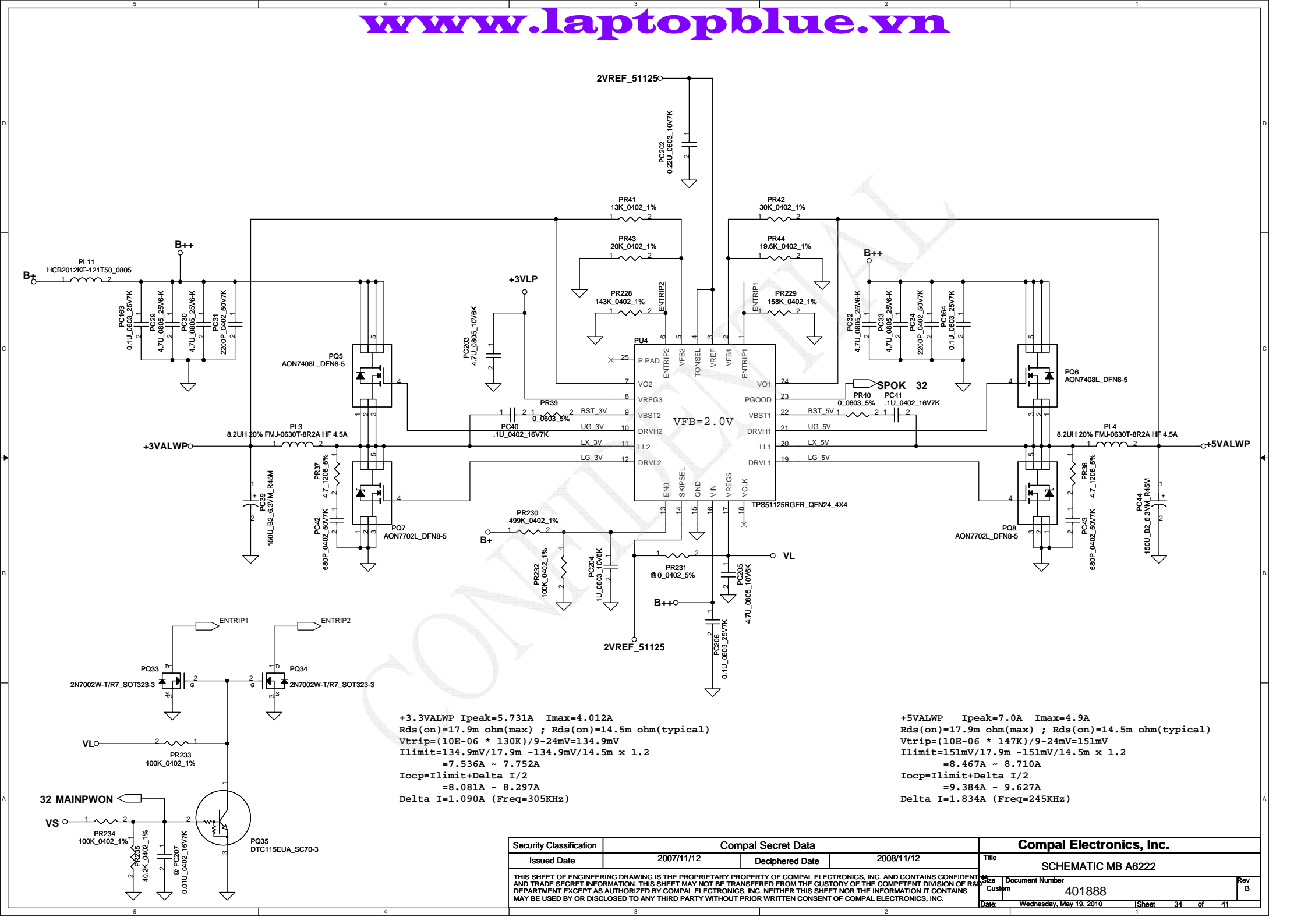
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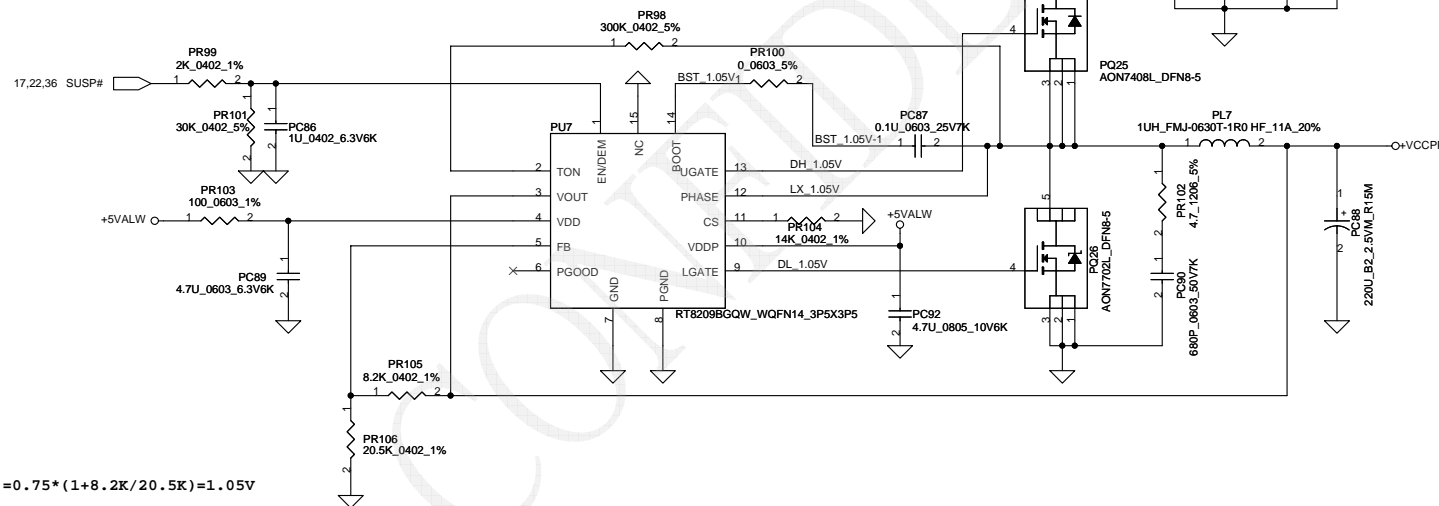
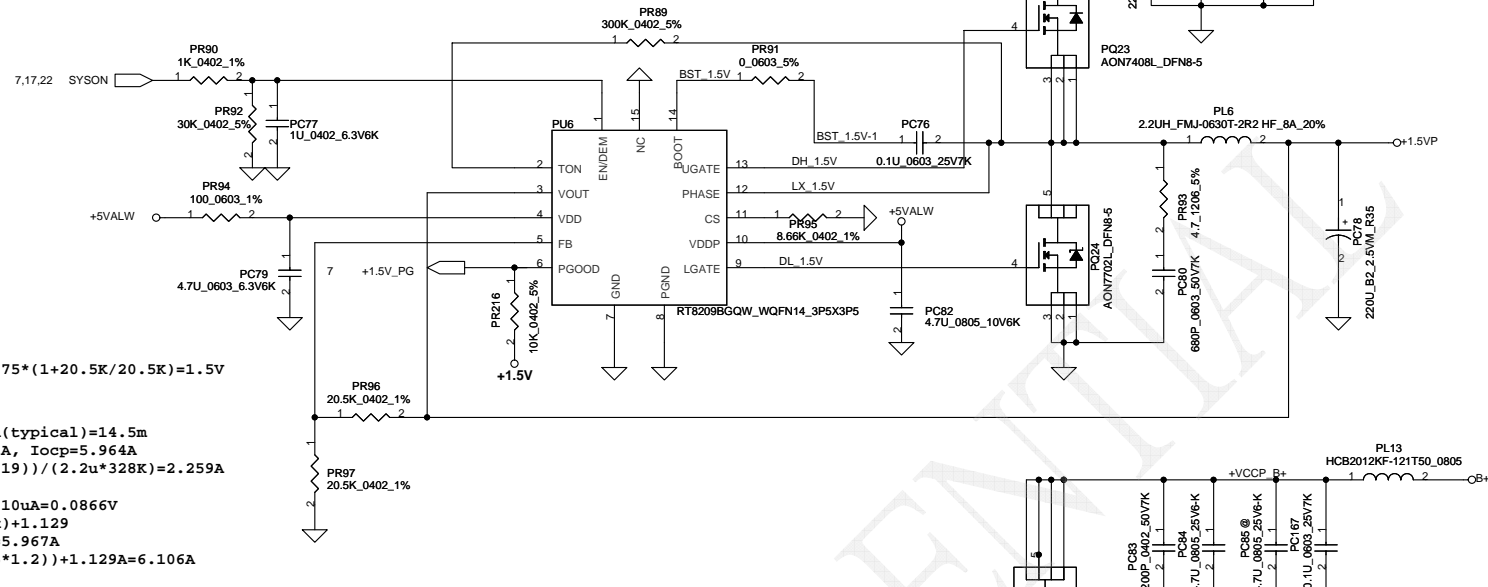


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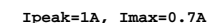
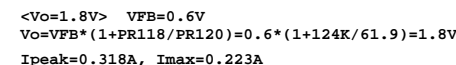
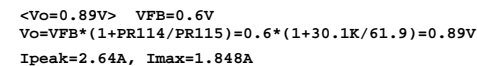
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C







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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Improve +1.8V efficiency	Fellow acer SPEC	0.1	36	Change PU10 from SA000034S00 (APL5930KAI-TRG_S08) to SA00003RU00 (SY8033BDBC_DFN10_3X3)	2010.1.25	EVT
2	Change +1.5V power good signal pull high voltage and net name	For HW request	0.1	35	Change +1.5V power good signal pull high voltage from 3.3V to 1.5V and net name change to DDR3_PG	2010.1.26	EVT
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	PU4 Pin25 change to no connect	modify for 3/5V load balance(TI FAE suggest)	0.1	34		2010.1.12	EVT
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

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<2009/4/28>
Update new power schematic,
release first version NAV50 schematic

<2009/04/29>
Add R1182 R1183 L3 on page 9
Change J3 to R1184 on page 13

<2009/04/30>
Change JDIM1 to SP07F001720 on page 7
Del SATA1 Port on page 12
Change R51 R57 R70 R63 R317 R314 R190 to 0402 Size on page 21

<2009/05/04>
Add WWAN_CLKREQ# and R107 pull-high to +3VS on page 8
Add CRT_DET# on page 10
Add CRT_DET# circuit on page 13
Add 3 LEDS on page 16
Add BT/BTN Board CONN. on page 16
Update TP/B CONN. to SP01000LB00 on page 19

<2009/05/11>
Add INVT_PWM on Page 5
Del R323 on page 5
C74 change to 2.2U_0603 on page 6
C267 change to 22U on page 6
C391 change to 0.1U on page 6
Del C67 C35 C33 C36 on page 6
Del +LGI_VID and U71.A21 direct connect to +VCCP on page 6
Follow Intel checklist, add R52 on FSB on page 8
Add D5 D7 D8 on page 4
Add R174 on page 9
Add PCI_RST# on page 11
Add C1115 C1114 C1116 C1117 C1118 on page 15

<2009/05/12>
Follow Intel Layout Checklist, Add C141 on VDDSPD on page 7
Modify SRC CLK PORT LIST on page 8
Del CLKREQ_LAN# on page 8
Change PCIE Port list on page 13
Change USB Port list on page 13
Add W/L 3G SW on page 16
Del R103 on page 18

<2009/05/13>
Change JMINI1 to PCIE Port 3 on page 15

<2009/05/14>
Page8 Change C174 C175 to 10U_0603

<2009/05/14>
Update New Power schematic
Del R376 R377 on page 8
Del D5 D7 D8 on page 4
Change JLVDS1 to SP010006810 on page 9
Add D6 for EMI on page 9
Change C1106 to C_0603 type on page 9
Change USB_OC# on page 13
Add USB Port2 on page 20
Change JP11 Pin define & Add D22 on page 19
Change C512 to 1u_0402 on page 15
Add U29 (MEDIA_LED#) on page 16

<2009/05/19>
Update new clock GEN co-lay schematic on page 8

<2009/06/05>
Update new clock GEN co-lay schematic on page 8
Follow Intel check list change C161 C165 to 27P on page 8
Follow Intel check list change C56 to 22uF on page 6

<2009/06/08>
Update New Power schematic 06/06 version
Page 13- a.Del R203 (pull-up GPIO6 Resister)
b.Change R1184 NU
Page 17- a. Add VGATE
b. Del R1294
c. Change D30 NU
d. Change R1295 to 0 ohm
e. Add R1309 0 ohm on EC_RSMRST#
f. Pull-up LAN_WAKE# +3VALW
g. ICH_POK change to PCH_POK
h. Pull-up KB_RST# to +3VS
Page 10- a. Add R1283 R1284 ,Change R247 R249 to 10 ohm
b. Add @ on U10 U11 C301 C298
c. Del C302 C300 R1281 R1287

<2009/06/11>
Page 7 Add R1184 NU
Page 22- Modify USB_OC#1_2 to USB_OC#2
Page 17- Modify PLTRST# to PCI_RST#
Page 17- Add @ on R1311

<2009/06/12>
Page4 Add C314 C313 C1150 D19 on +VCC_FAN1
Page8 Add C1145 C1146 C1147
Page10 Move CRT_DET# from Page13 to Page10
Page13 Add +RTCVCC circuit

<2009/06/15>
Update New Power schematic (change PBJ1 to PJP3)
Page 10 modify C310 C308 C303 C307 C306 C304 Bom Structure
Page 22 Modify Hole location by (ME drawing 06/12)

<2009/06/16>
Page7 Modify DDR Command Control Pin pull-high Resister location
Page9 Change R577 to 0402 type

<2009/06/17>
Update New Power schematic 06/17
Page9 modify LVDS Conn. Pin define
Page9 Del C1110
Page4 Add EMI solution D38 D39 D40

<2009/06/18>
Update New Power schematic 06/18
Page8 modify U4 Pin define and Q31
Page13 Add R1376, R1377
Page15 Modify C403
Page23 Modify H11

<2009/06/19>
Page4 Add new signal CPU_ITP , CPU_ITP#
Page5 ADD R1378
Page6 ADD C1152,C1153,C1154 C1160,C1161,C1162
Page7 DDR_A_D8與DDR_A_D9互換
Page8 ADD R1379,R1380,U77,R1381,C1157,R1382,R1383,R1384,C1157
Page8 DEL C390
Page9 ADD C1156
Page11 DEL R1322, R1154
Page13 DEL U77, ADD C1158
Page17 ADD C1159

<2009/06/22>
Page22 change IO Conn. pin34 from 48M to USB_ON#
Page10 change JCRT1 P/N to SP010906182

<2009/06/23>
Page15 Add C1163 C1164 C1165 C1166
Page18 change PWR/B Conn. P/N to SP01000H300
Page22 change JUSB1 JUSB2 P/N

<2009/06/24>
Page8 Change C1350 C1351 to 0402 type
Page10 Add R1385 R1386 on JVGA_HS JVGA_VS

<2009/06/25>
Page22 move some parts to I/O Board , Add the MONO_IN_R on M/B

<2009/06/29>
Page16 Change JP24 to ACES_88266_05001
Page15 Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T

<2009/06/30>
Page18 Change PWR_LED# to PWR_PWM_LED#
Page17 Add PWR LED DETECT PIN on Pin97

<2009/07/02>
Update New Power schematic 07/02
Page9 Add C1167 C1168 for RF request.
Page13 Change R223 to 100K
Page16 change JP24 to ACES_85201-0505N
Page17 Del R1387 R1388 on EC Pin97
Page17 Add New Board ID to separate NAV50 NAV60
Page17 Change 展頻IC to SA00003J400 (New)
Page18 Add D41 for ESD

<2009/07/03>
Page 11 Add R1184 NU to PWR_PWM_LED#
Page8 Change co-lay net name to +1.5VM_CK505
Page20 Change JP2 Pin42 to +5VS

<2009/07/06>
Page18 Add pwr switch for NAV50

<2009/07/08>
Page5 Add 470pf on H_SMI# for known issue.

<DVT START>

<2009/08/04>
Page5 CLK_CPU_HPLCLK CLK_CPU_HPLCLK# exchange
Page9 Change JLVDS1 to P/N ACES 88341-3001 30P
Page17 del PM_1.8V(U6.82) ,Del R1310 R1311
Page18 Del D41

<2009/09/03>
Page7 Change C112 to 0402 type
Page8 Add T6 on CLK_48M_CR
Page16 Modify JP18 Pin define change +5VALW +5VS to +3VALW +3VS
Page20 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7
Page21 Del H12

<2009/09/08>
Update Power schematic 0904
Page18 Change R1388 to 100 ohm 0402
Page18 Change LED1 to SC591NB5A00

<2009/09/10>
Update Power schematic 0910
Page22 unmount Q6 Q8

<2009/10/07>
Page4 U71 Change to SA00003M800
Page6 R26 Change to SHI00009C00
Page13 R152 Change to SD034200A80
Page18 R1388 Change to SD028510A80

<2009/11/26>
Page13 H_STP_PCI# Pull high to +3VS
Page9 change JLVDS.27 to disconnect
Page9 Add DMIC_CLK & DMIC_DATA in JLVDS
Page20 Add DMIC_CLK & DMIC_DATA in JP2.10 & JP2.12
Page15 Change R504 Bom structure to @ .

<2009/11/30>
Page21 change H20, H11 footprint

If I have revised anything ,
I will high light by pink word and pink frame.

04/30
(1) P2 Add CLK_SD_48M

05/05
(1) P2 update compal number
(2) P2 Add USB_OC#1_2 and USB_ON# to net
(3) P3 Add U2 circuit
(4) P3 Add IC(U2)
(5) P4 Revised 0 ohm
(6) P5 Add digital MIC

05/12
(1) P2 Update information about aperture
(2) P2 Update USB connector
(3) P3 Revised net name
(4) P5 Revised circuit
(5) P7 Upate RJ45 connector (the same as KAV60)
(6) P8 Update WLAN connector(the same as KAV60)

05/14
(1) P3 Deleted JUSB2
(2) P7 Update RJ45 connector(the same as NAV20)

05/20
(1) P2 Update connector pin name

06/01
(1) P7 Update circuit
P8 Revised 37、39、41、42、43 to NC

06/12
(1) P8 Update connector to DC040006S00

06/19
(1) P6 Update Headphone connector to SP010906161
(2) P6 Update MIC connector to SP010906161

06/23
(1) P3 Update USB connector to SP010906181
(2) P2 Add connector(JP21)_delete

06/26
(1) P2 Add circuit
(2) P8 Update JMINI1 footprint

07/01
(1) P2 Update pin number 8,10,14,16,20,22
(2) P8 update pin 23,25,31,33

07/02
(1) P2 Update PIN42 to +5VS
(2) P7 Add R42

07/02/B
(1) P4 Update JP1

07/04
(1) P5 Add C23

08/06
(1) P4 Add R32、R33
(2) P4 Add R1347、R1348

10/07
(1) P3 DEL R1, R2 ; ADD L1
(2) P4 Change C1065, C1068 to SE071270J80
(3) P5 Change R441, R438 C1068 to SM01000FO00
(4) P6 D29, D30 NU

12/01 delete JP4.2、JP4.3
12/01 move D17 C603 C604 to page 2

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